

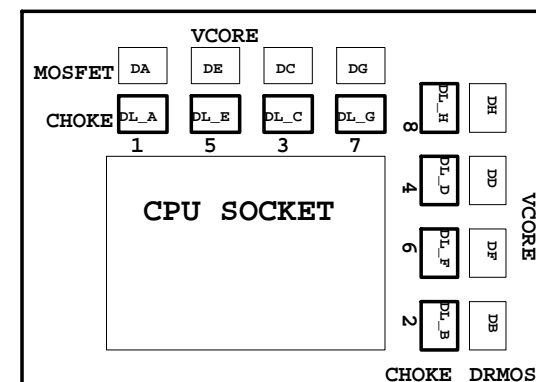
Model Name: GA-Z87X-D3H Rev 1.1

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS X8 SLOT
16	PCI EXPRESS X16 SWITCH
17	PCIEX1*3 , PCIEX4 SLOT
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS , TPM SLB9635TT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	ITE8892 PCI BRIDGE
24	PCI SLOT
25	FUSB 3.0
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET TITLE

28	F_PANEL , F_USB2.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	LAN INTEL i217
32	DVI
33	HDMI , R_USB30
34	TABLE LIST
35	IR3563B_PWM
36	IR3550-VCORE
37	IR3570_DDR PWM
38	IR 3598-DDR
39	D720210 4port_Hub
40	D720210 4port_Hub POWER
41	D720210 4port_Hub_B
42	D720210 4port_Hub_B POWER

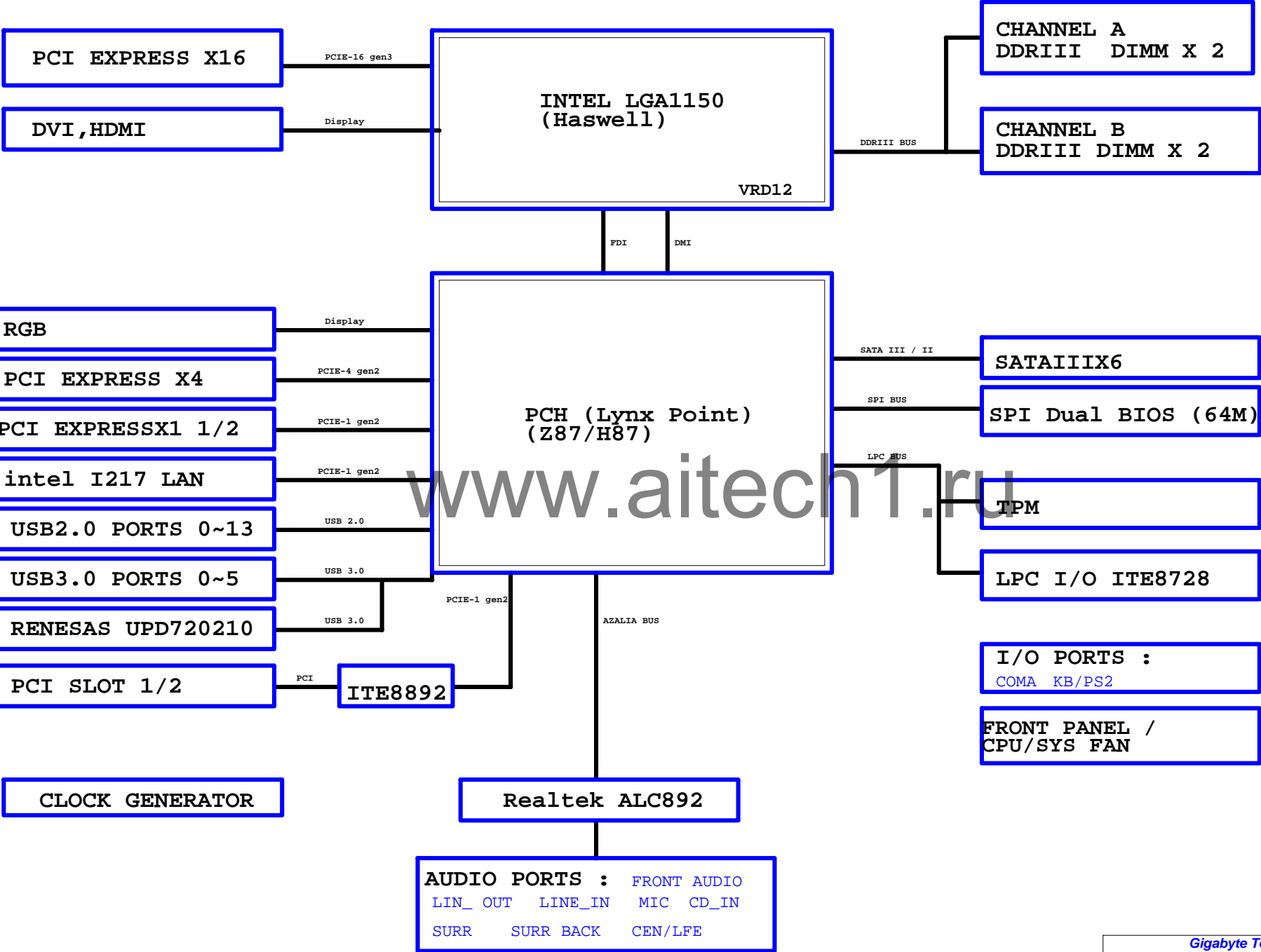


Component value change history

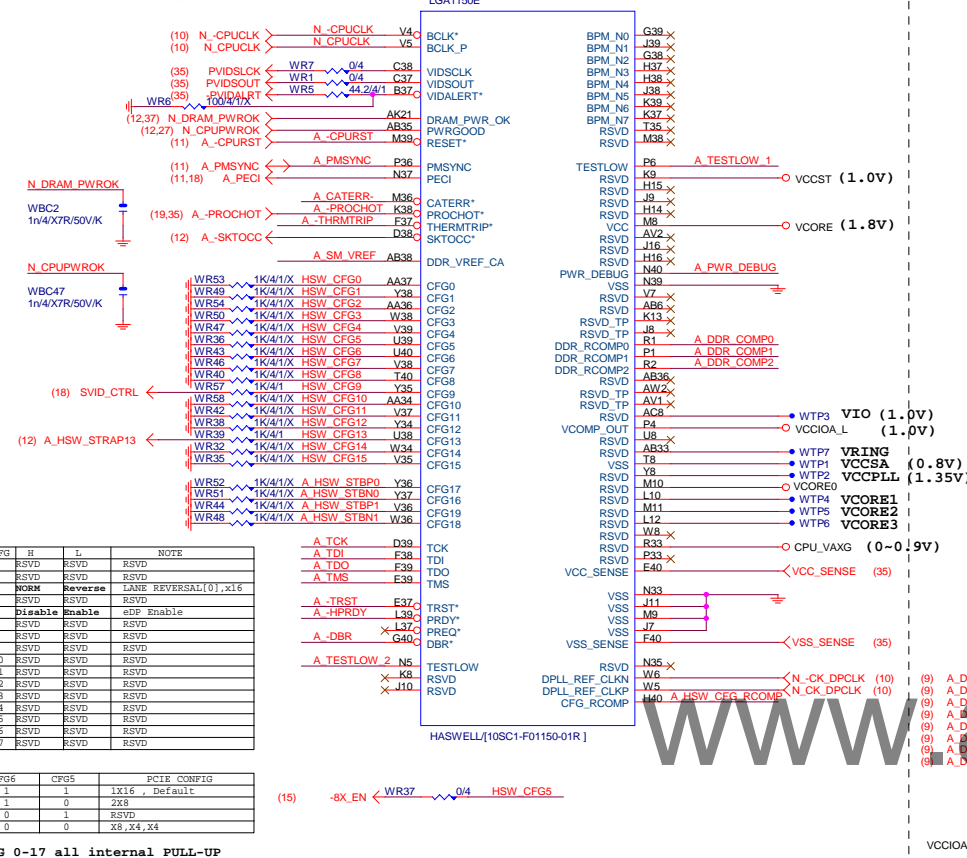
[illegible]

DATE	Change Item	Reason
2012/11/23	1. Change from Z87-D3H-02.DSN	Rev 0.1
2013/01/11	1. Change from Z87X-D3H_R01_1224B.DSN 2. PCIE_X4 clock change to PCIE_5 3. PCIE_X1_1 clock change to PCIE_3 4. PCIE_X8 clock change to PEG_B 5. N_PCIE_4_SW change to N_GPIO48 6. -PCIE_X1_PR3 change to N_GPIO22 7. Update Note 33, TI H/W charger	Rev 0.2
2013/03/28	1. Add net N_-SLP_A 2. CLR_CMOS 文字面修改 3. 所有的FAN 加0.1u/4, 要非常靠近FAN connect pin 2	Rev 1.01
2013/06/26	1. 只修改文字面版本 Rev 1.1 (For PCH C2 chip)	Rev 1.1

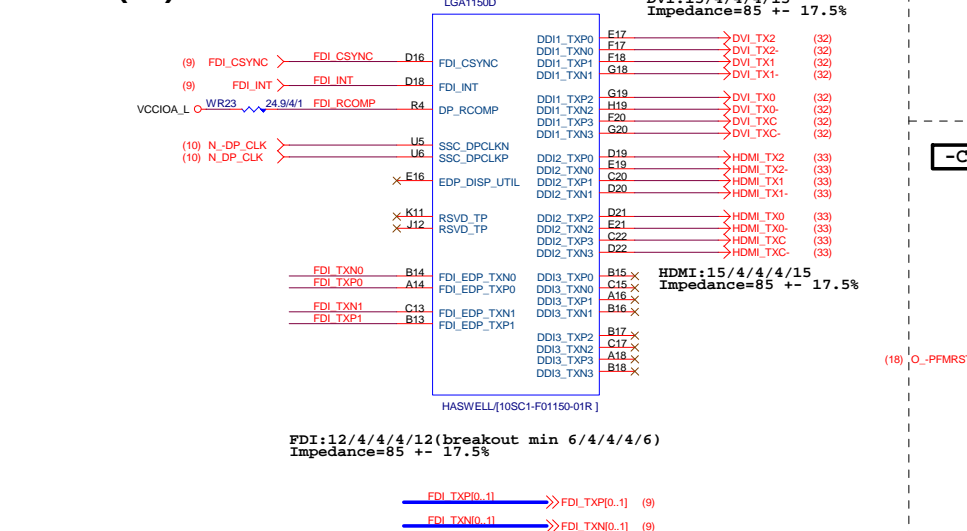
BLOCK DIAGRAM



LGA1150 (E)



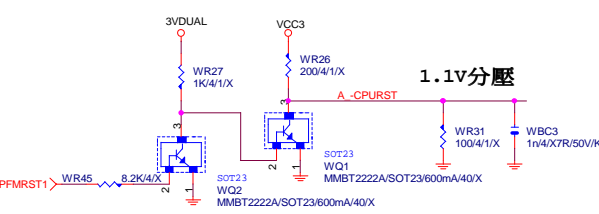
LGA1150 (D)



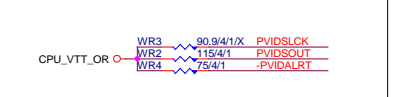
LGA1155 (C)



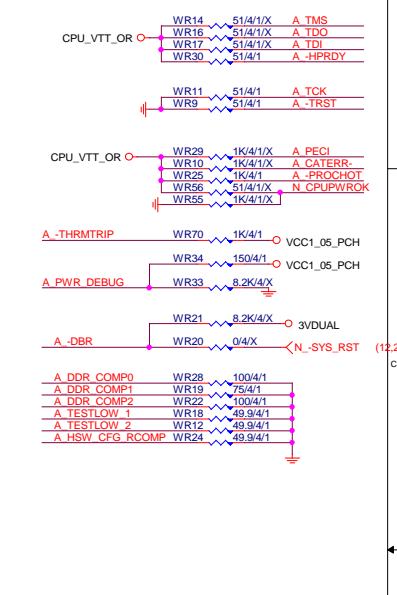
-CPURST



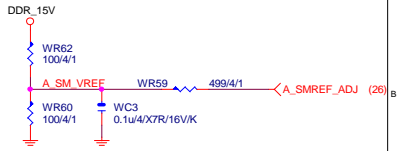
CPU SVID



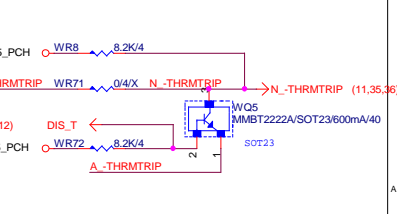
CPU PU/PD



SM REF



THRMTRIP DISABLE



Gigabyte Technology

CPU LGA1150-A			
GA-Z87X-D3H			
Size	Custom	Rev	1.1
Date	Monday, July 22, 2013	Sheet	4 of 43

(A)

LGA1150A

HASWELL/I10SC1-F01150-01R 1

(B)

LGA1150B

(CR)

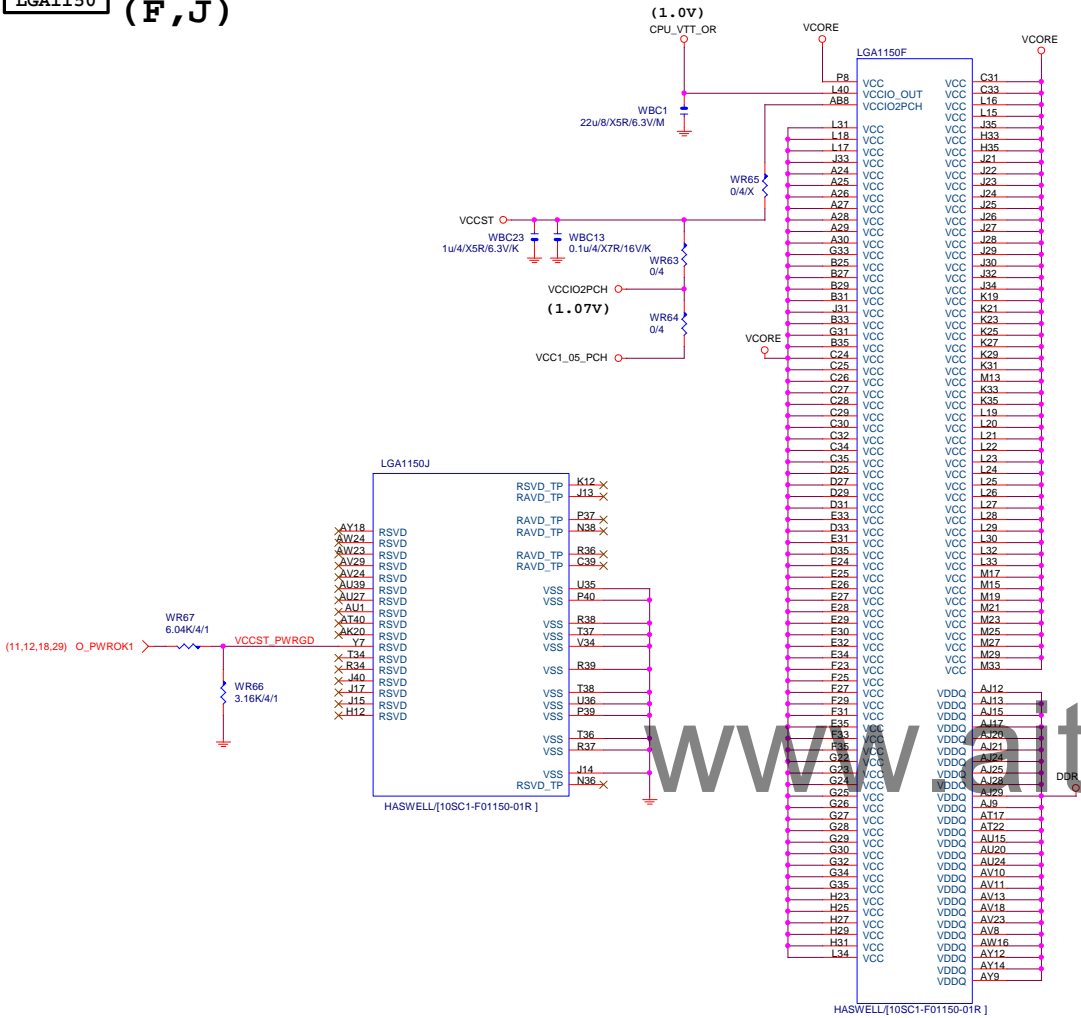
DDR BUS

(7)	MODT_A[0..3]	↔	MODT_A[0..3]
(8)	MODT_B[0..3]	↔	MODT_B[0..3]
(7)	MDA[0..63]	↔	MDA[0..63]
(8)	MDB[0..63]	↔	MDB[0..63]
(7)	DQSA[0..7]	↔	DQSA[0..7]
(7)	-DQSA[0..7]	↔	-DQSA[0..7]
(7)	MAAA[0..15]	↔	MAAA[0..15]
(8)	MAAB[0..15]	↔	MAAB[0..15]
(8)	DQSB[0..7]	↔	DQSB[0..7]
(8)	-DQSB[0..7]	↔	-DQSB[0..7]

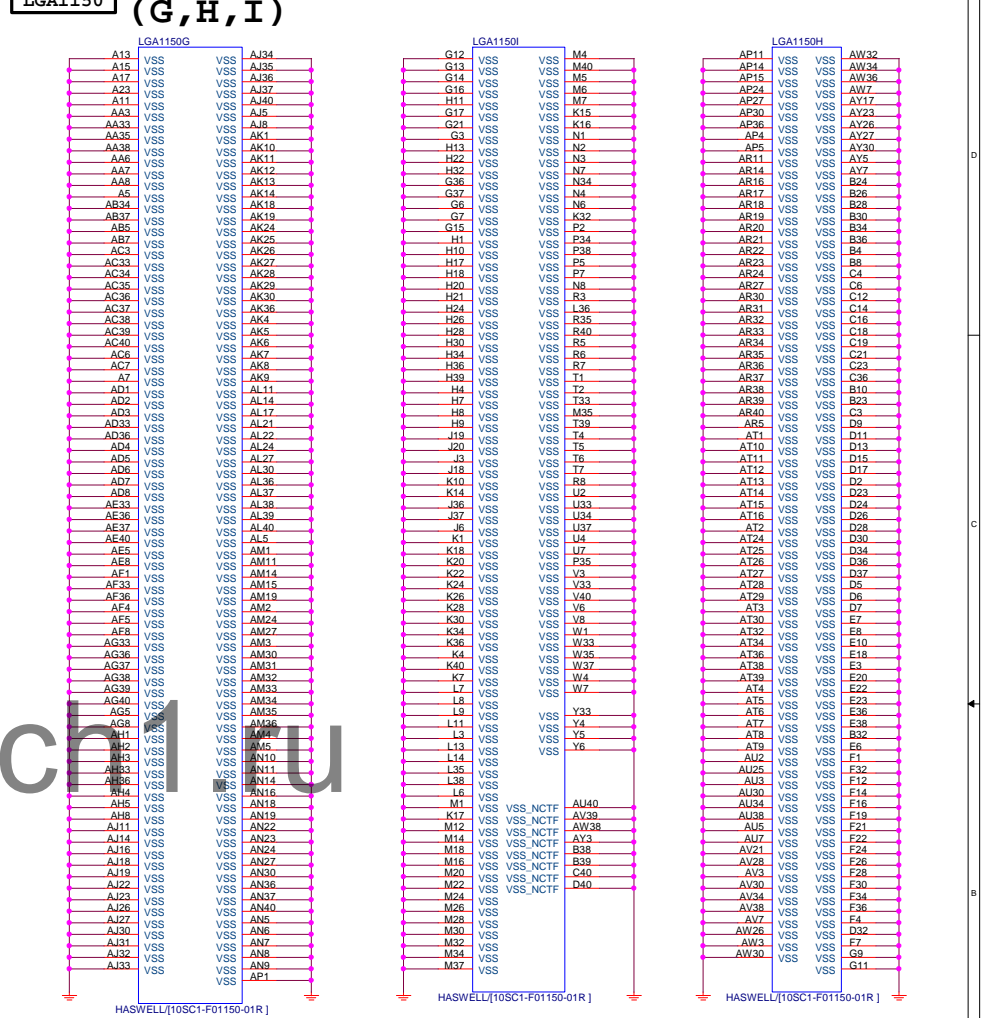
Gigabyte Technology

Title			
CPU LGA1150-B			
Size	Document Number	Rev	
Custom	GA-Z87X-D3H	1.1	
Date:	Monday, July 22, 2013	Sheet	5 of 43

LGA1150 (F,J)

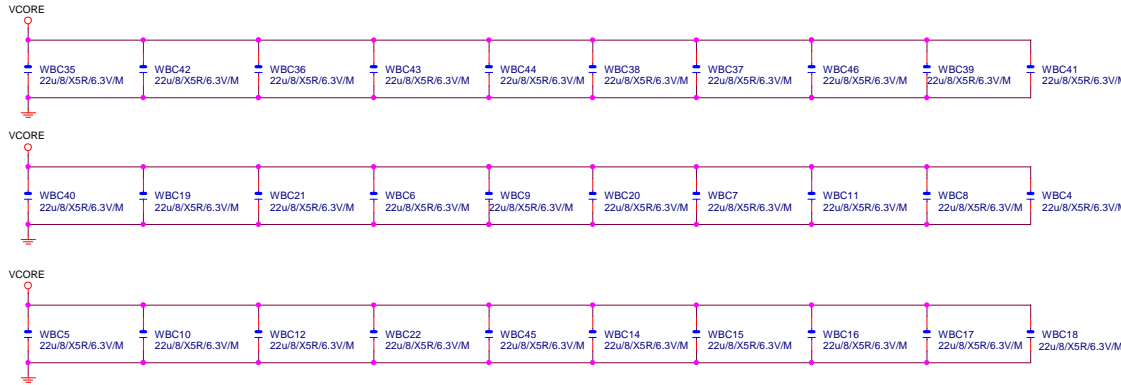


LGA1150 (G,H,I)



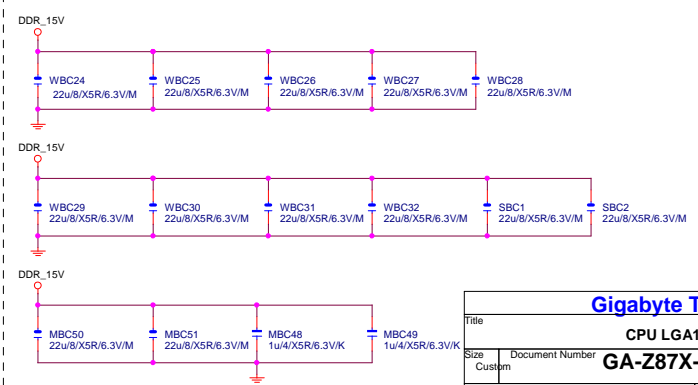
VCore CAP

(X30)



DDR CAP

(X15)

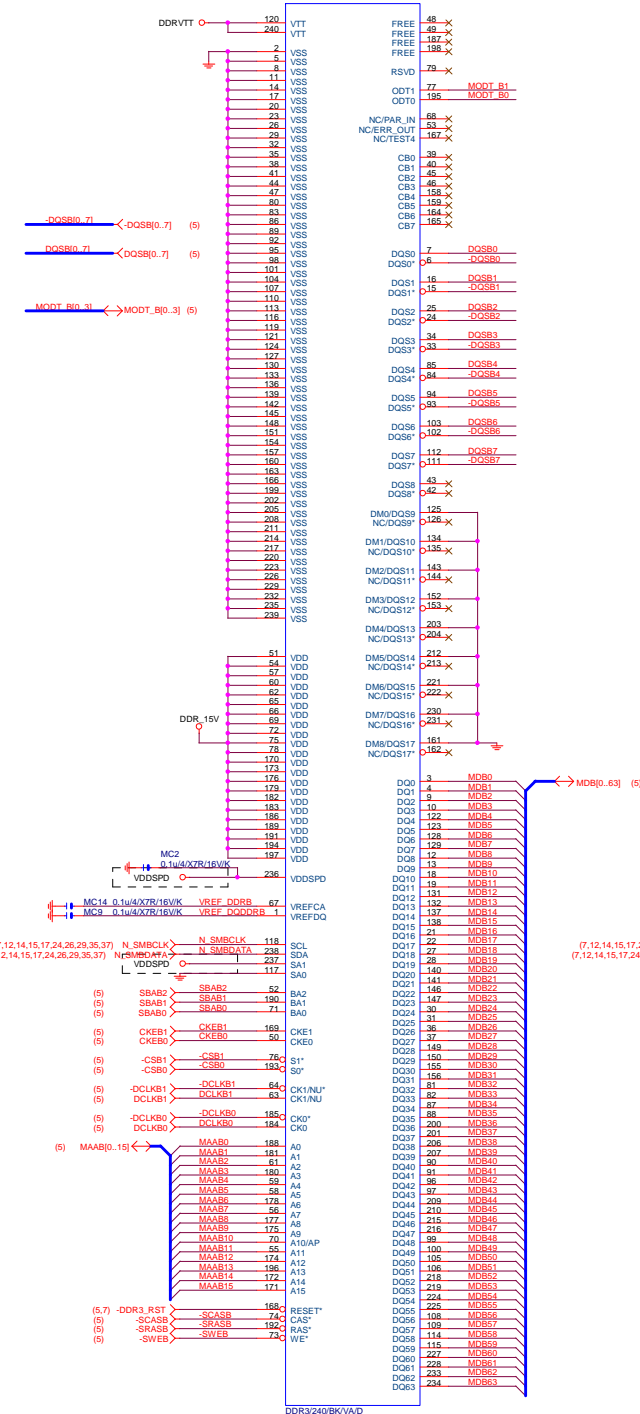


Gigabyte Technology

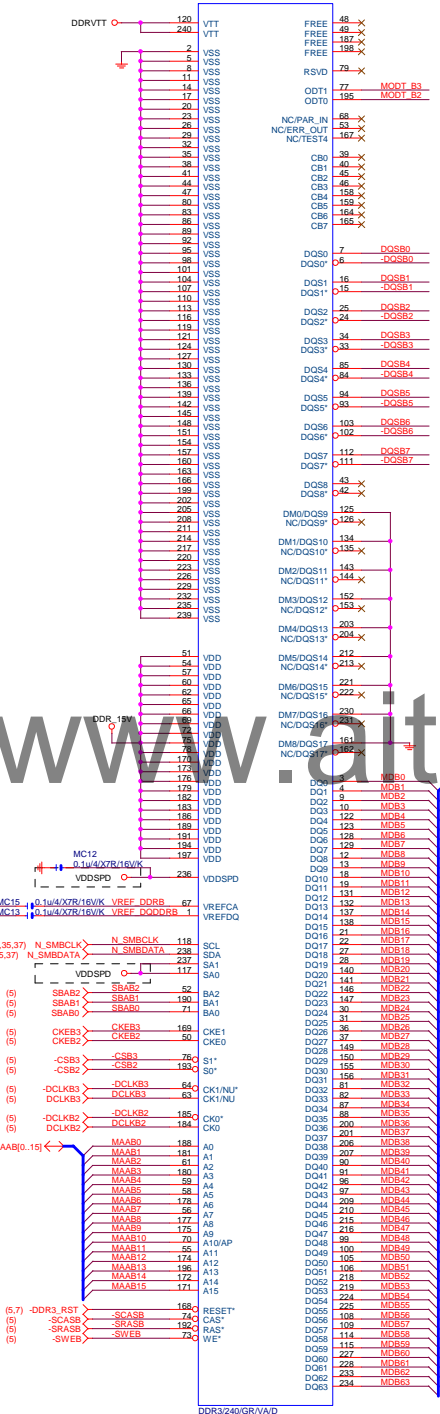
Title				
CPU LGA1150-C				
Size	Document Number	GA-Z87X-D3H		Rev
Custom				1.1
Date:	Monday, July 22, 2013	Sheet	6 of 43	

DDR3

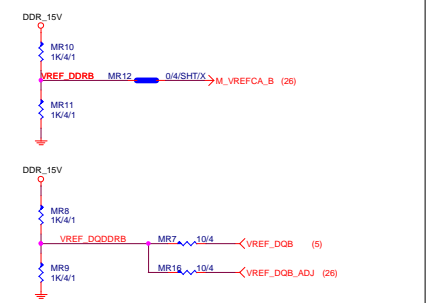
(B)



DDR3



DDR3 VREF



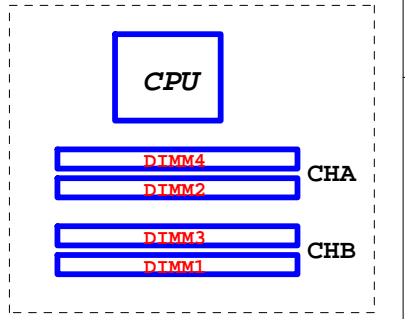
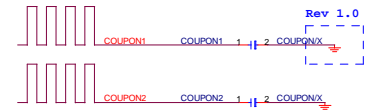
DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ
DDR3 clock=533MHZ
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

DDR3 1333MHZ
DDR3 clock=667MHZ
DDR3 single channel bandwidth=10.6GB/s
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ
DDR3 clock=800MHZ
DDR3 single channel bandwidth=12.8GB/s
DDR3 dual channel bandwidth=25.6GB/s

COUPON

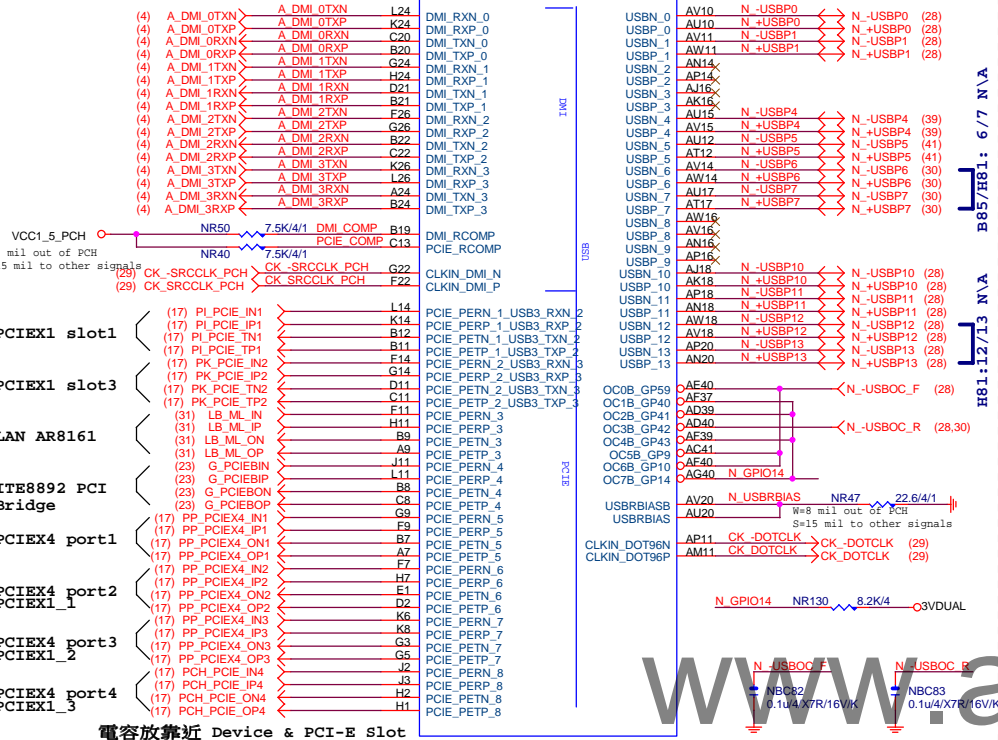


Gigabyte Technology			
Title			
DDR3 CHANNEL B			
Size			
Custom			
GA-Z87X-D3H			
Date			
Rev			
1.1			

PCH (B)

DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

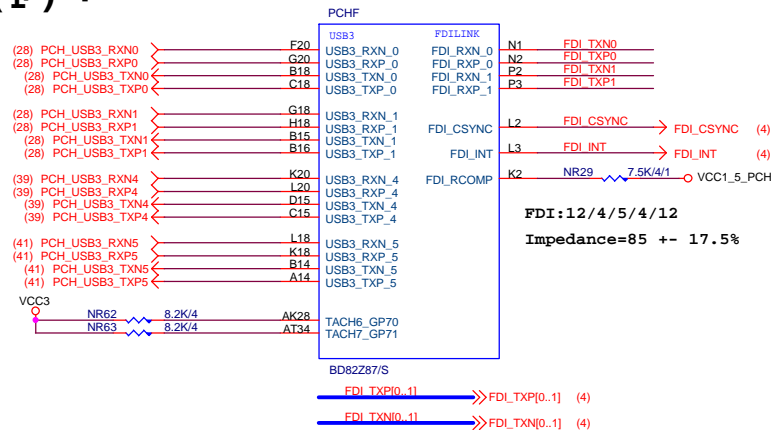
USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%



PCIEI1:15/4/4/15 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

PCH (F)

USB3.0 : 20/5/7/5/20 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

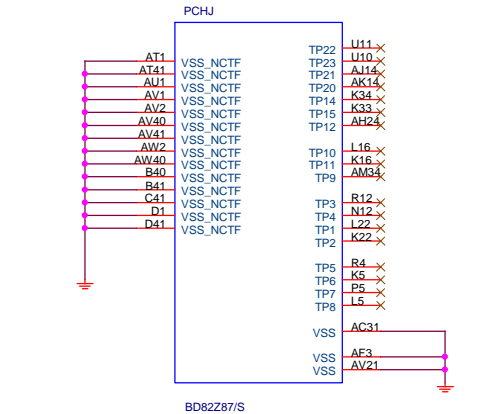


USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

Mount for integrated clock Generation Mode

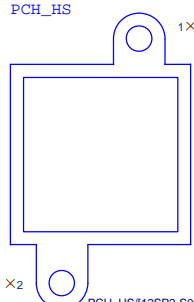
CK_DOTCLK NR92 8.2K/4
CK_DOTCLK NR91 8.2K/4
NR92 short to GND in non graphic SKU

PCH (J)



PCIEI1:15/4/4/15 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

PCH H/S



USB TABLE

OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

USB OC#	Configure
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

Gigabyte Technology

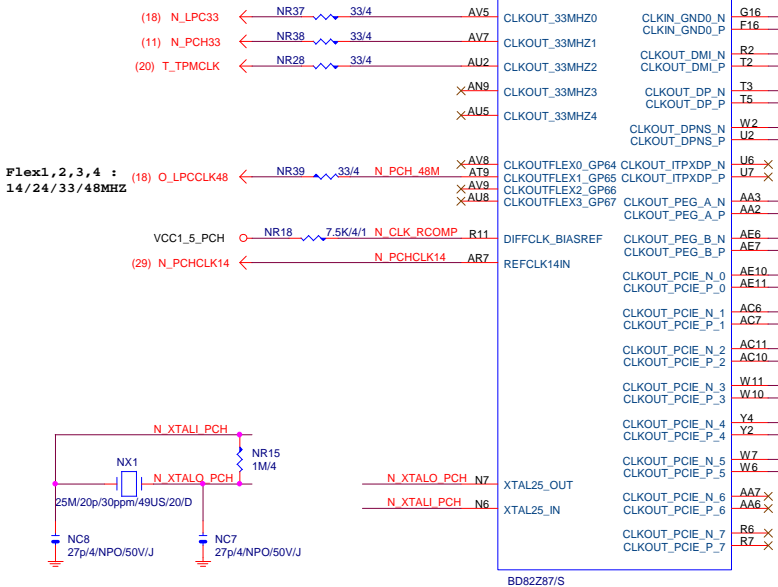
Title: PCH FDI,DMI,USB,PCIE

Size: Custom Document Number: GA-Z87X-D3H Rev: 1.1

Date: Monday, July 22, 2013 Sheet: 9 of 43

Pin	Function	Pin	Function
AJ2	DDPB_HPD	AH3	H SYNC
AH5	DDPC_HPD	AH2	V SYNC
AJ4	DDPD_HPD	NR26	33/4 N_GHSYNC
		NR33	33/4 N_GVSYNC
	VGA_RED	AC2	N R
AK6	DDPB_AUXN	AE2	N G
AK8	DDPB_AUXP	AC3	N B
AG7	DDPC_AUXN		
AG6	DDPC_AUXP	AG4	N DDCDATA
AG11	DDPD_AUXN	AL3	N DDCCLK
AG10	DDPD_AUXP	AL2	N DDCCLK
	VGA_IRTN	AF5	N VGA RSET NR34
	VGA_DDC_DATA		649/4/1
	VGA_DDC_CLK	AN3	N DDPD_CTRLCLK
	DAC_IREF	AM2	N DDPD_CTRLCLK
	DDPC_CTRLCLK	AM1	N DDPD_CTRLCLK
	DDPB_CTRLCLK	AJ5	N DDPB_CTRLDATA
	DDPB_CTRLDATA	AN4	N DDPB_CTRLDATA
	DDPD_CTRLCLK	AN2	N DDPB_CTRLDATA
	DDPD_CTRLDATA		

BD92287/S



NR42 8.2K/4
NR41 8.2K/4

SSOP6_ESD

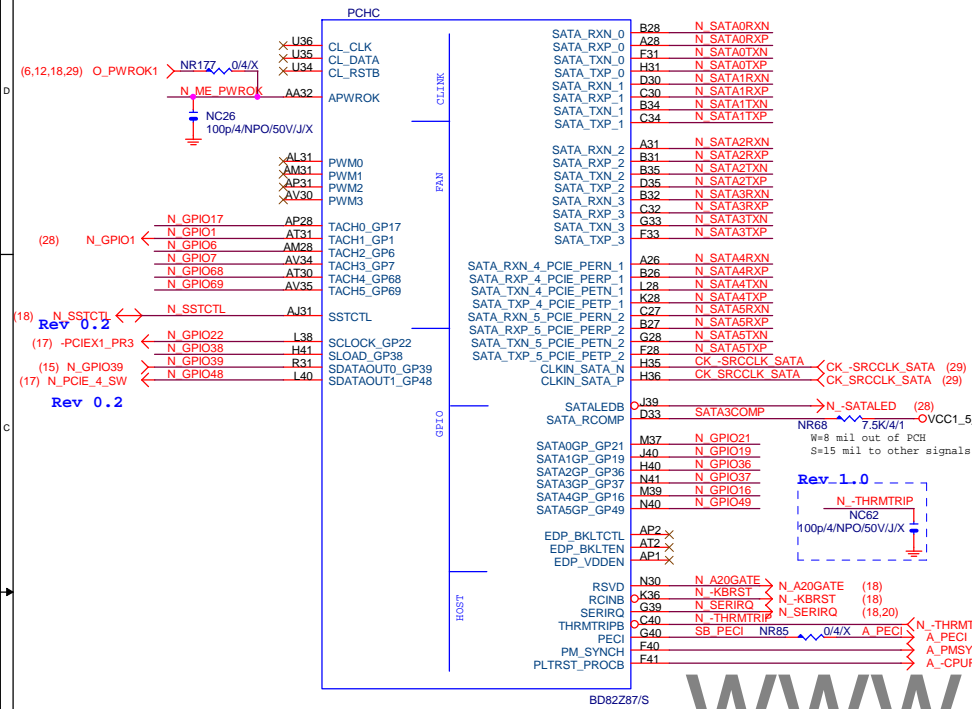
ESD4

Schematic diagram of the DDC interface circuit. It shows two 74VHC04 inverters (Q47 and Q48) connected between the N_DDCDATA and N_DDCCLK signals and the VGADDDCDA and VGADDDCLK signals. Each inverter has a 2N7002/SOT23/25pF/5 MOSFET at its input and output. The input resistors R146 and R147 are 2.2K/4/1, and the output resistors R144 and R145 are 2.2K/4/1. The circuit is powered by VCC3 and ground.

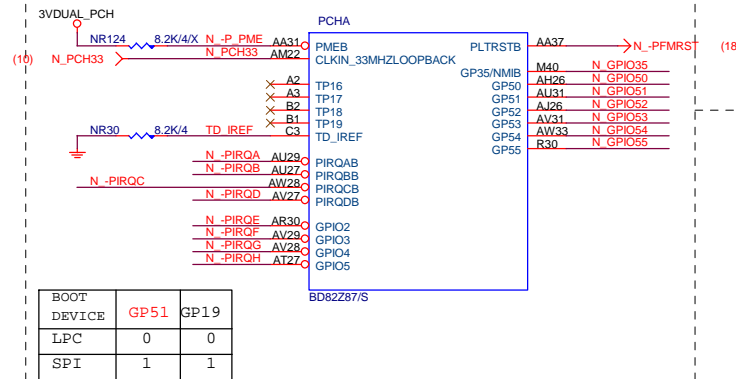
Title				PCH DISPLAY ,CLK BUFFER				Rev	
Size		Document Number						1.	
Custom		GA-Z87X-D3H							
Date: Monday, July 22, 2013				Sheet		10		of 43	

(C)

SATA3 : 20/5/4/5/20 (breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

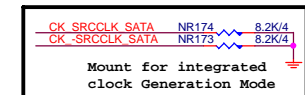


PCH (A)

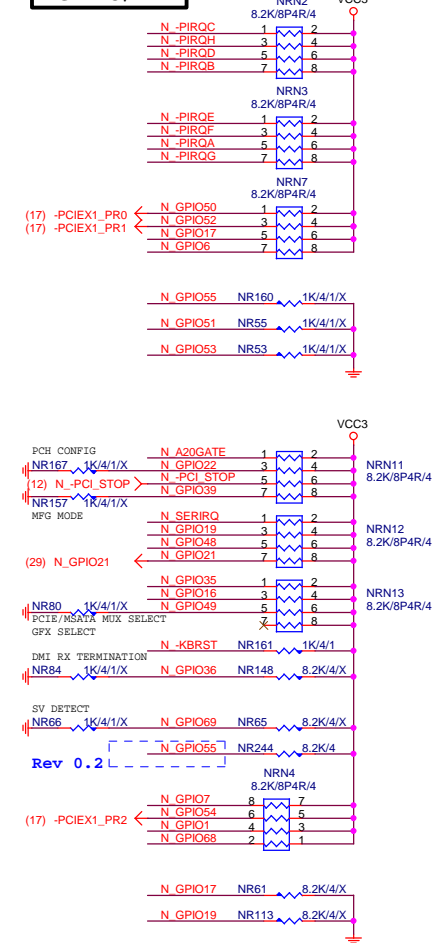


```
Default int pull up on GP51,
Default SPI boot devices
```

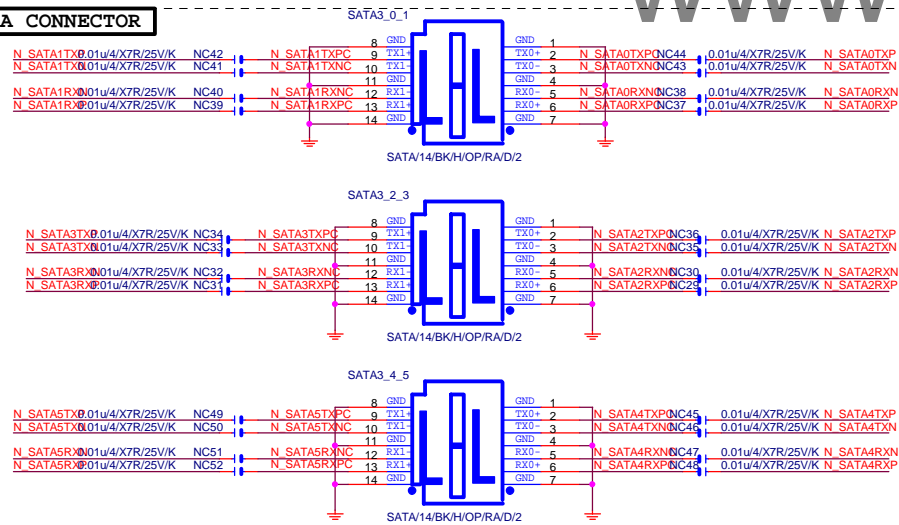
PCH CLK PD



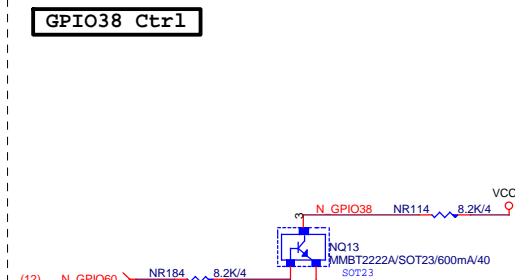
PCH PU/PD



SATA CONNECTOR



GPIO38 Ctrl



Gigabyte Technology

Title			
PCH HOST , SATA, PCI			
Size	Document Number	Rev	
Custom	GA-Z87X-D3H	1.1	
Date:	Monday, July 22, 2013	Sheet	11 of 43

(D)



MEY-NE



```

|-----|
|At least 10ms delay after|
|3VDUAL PCH stabel      |
|-----|

```



GP8:Low to enable



GA-Z87X-D3H

Date: Monday, July 22, 2013 Sheet 12 of 43

32.768KHZ

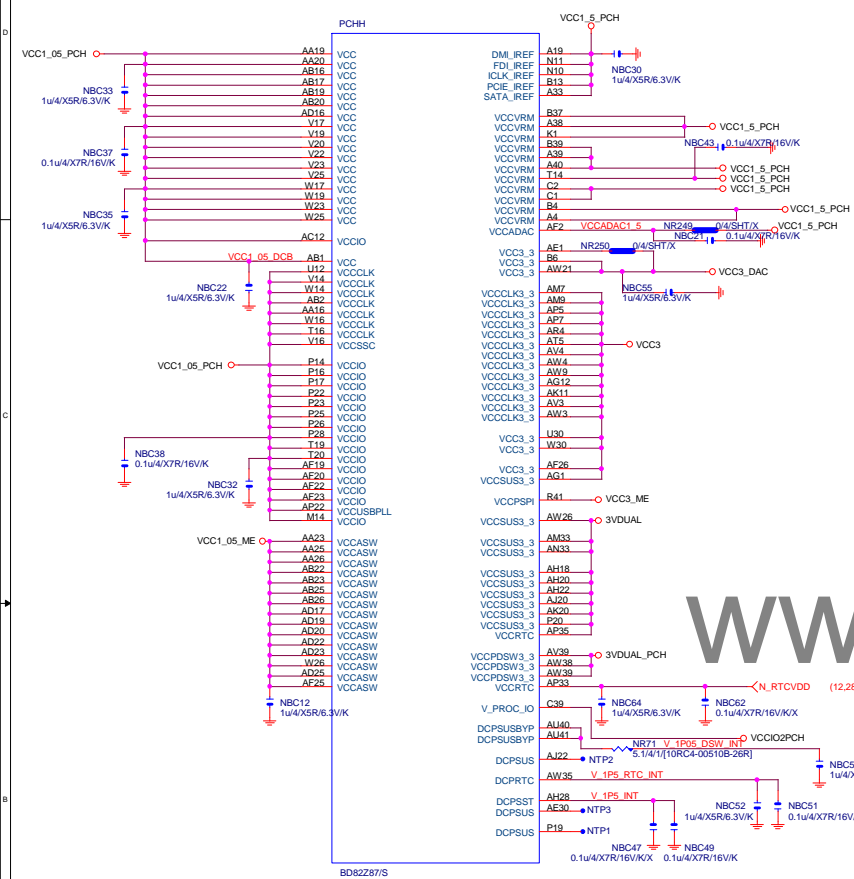


CLR_CMOS

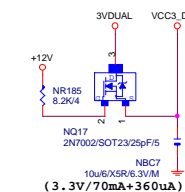
N - R

PH/1*2/BK/2

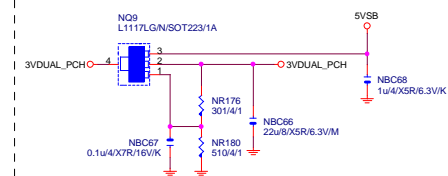
PCH (H)



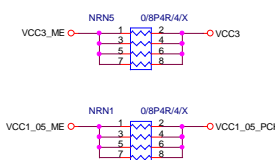
VCC3_DAC



3VDUAL_PCH



SHT PWR



CAP

(3.3V) (X6)

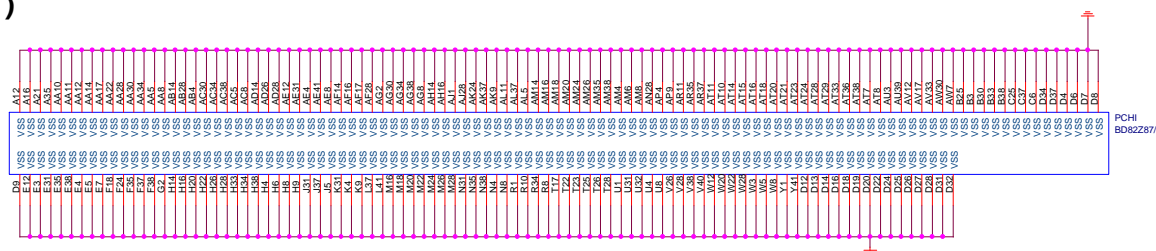
(1.05V) (x5)

(1.05V) (x6)

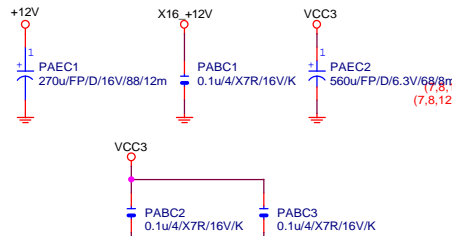
$$(1.05V)(x2) \quad (3.3V)(x2)$$

(1.5V) (x10)

PCH (I)

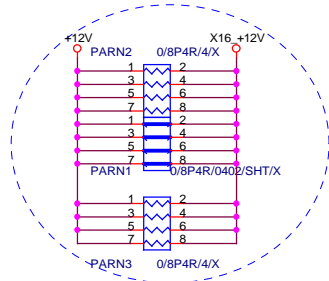


PCIEX16 CAP



PCIEX16 PROTECT SHT

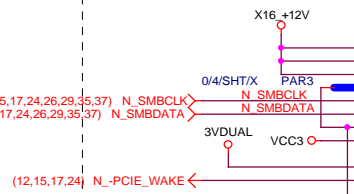
+12 protect short-wire test



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4X5R/6.3V/K	PA EXP SW TXN15 C

PCIEX16 SLOT



PA EXP TXP0 C
PA EXP TXN0 C

PA EXP TXP1 C
PA EXP TXN1 C

PA EXP TXP2 C
PA EXP TXN2 C

PA EXP TXP3 C
PA EXP TXN3 C

PA EXP TXP4 C
PA EXP TXN4 C

PA EXP TXP5 C
PA EXP TXN5 C

PA EXP TXP6 C
PA EXP TXN6 C

PA EXP TXP7 C
PA EXP TXN7 C

PA EXP SW TXP8 C
PA EXP SW TXN8 C

PA EXP SW TXP9 C
PA EXP SW TXN9 C

PA EXP SW TXP10 C
PA EXP SW TXN10 C

PA EXP SW TXP11 C
PA EXP SW TXN11 C

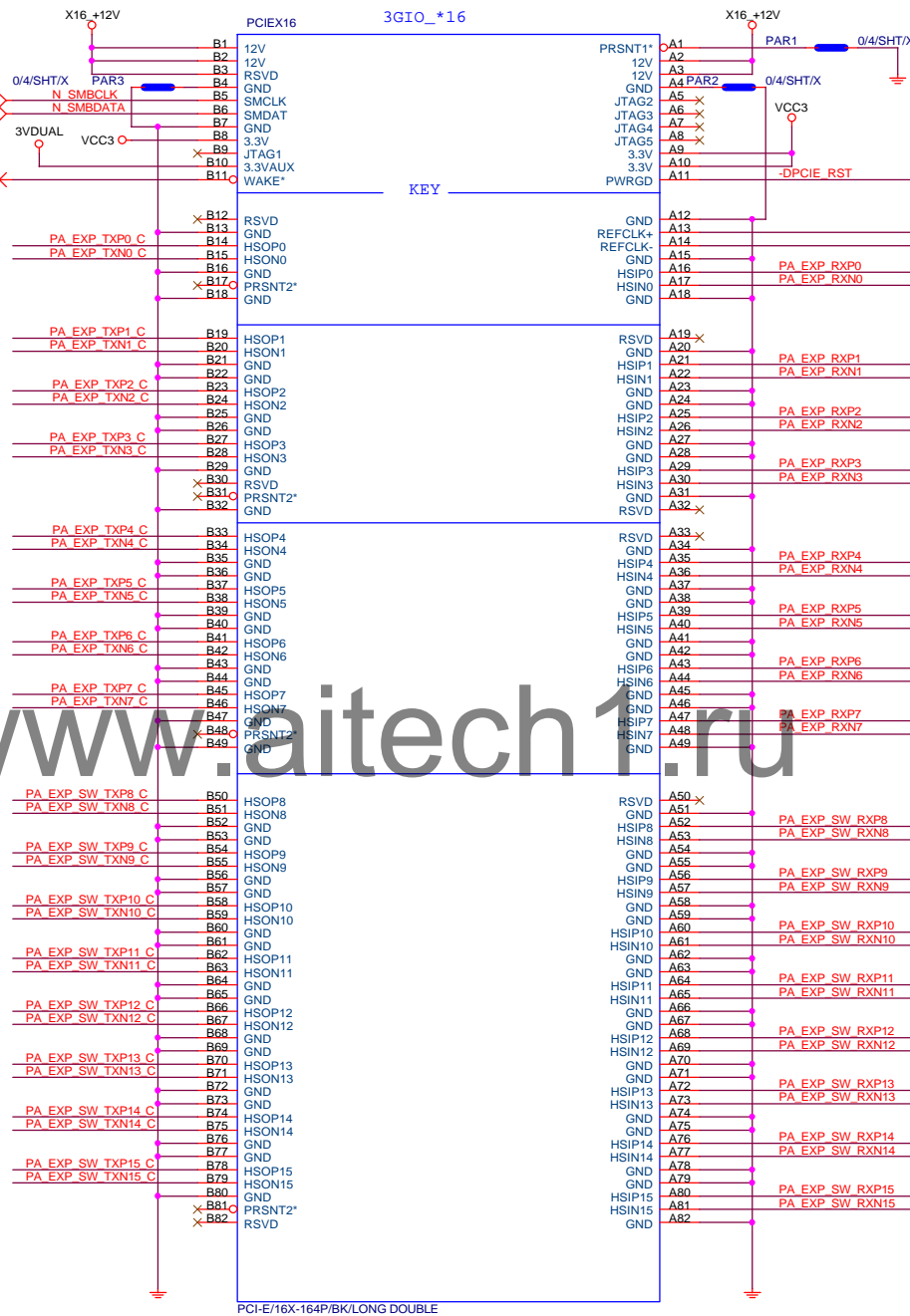
PA EXP SW TXP12 C
PA EXP SW TXN12 C

PA EXP SW TXP13 C
PA EXP SW TXN13 C

PA EXP SW TXP14 C
PA EXP SW TXN14 C

PA EXP SW TXP15 C
PA EXP SW TXN15 C

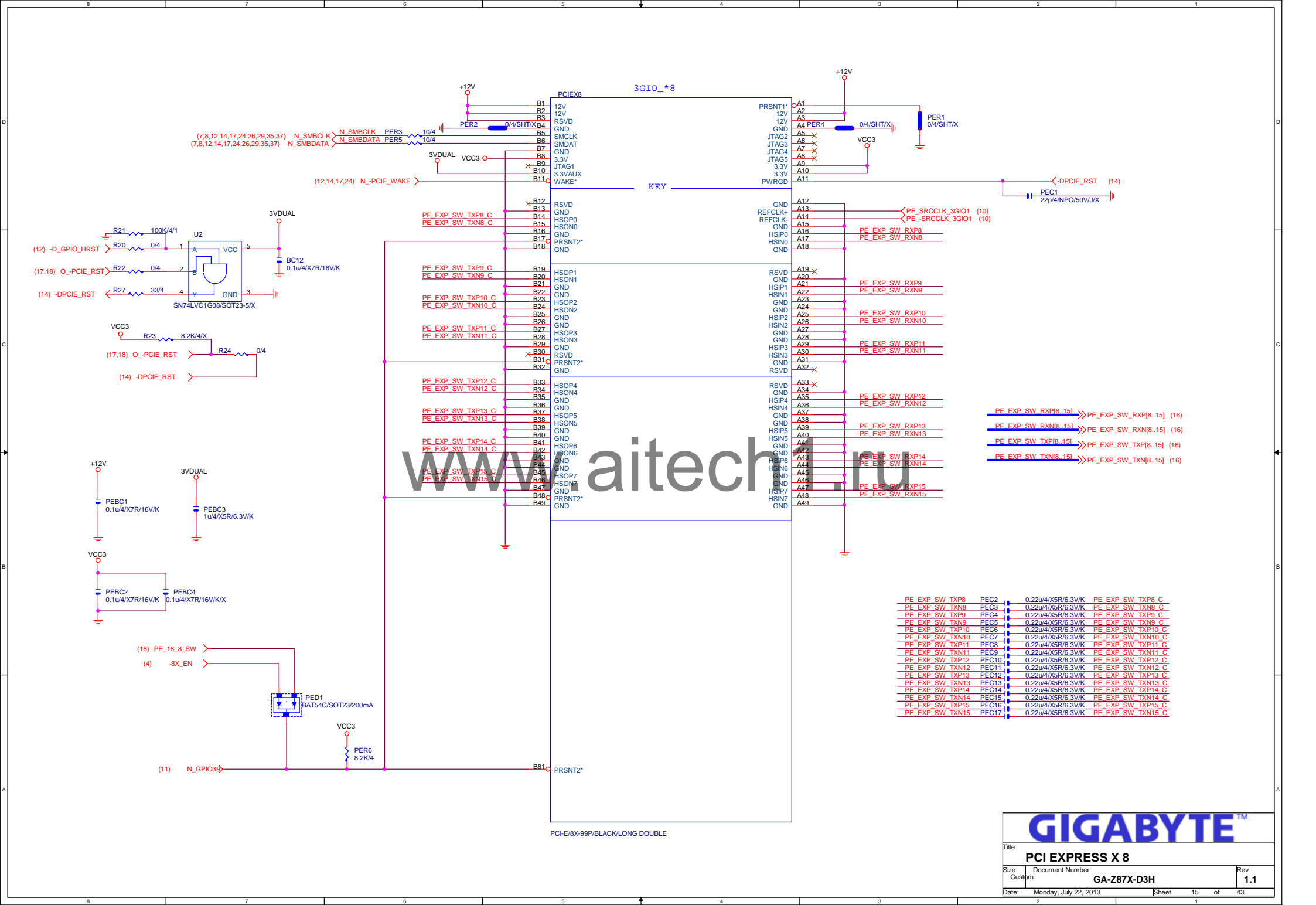
PCIESLOT-164DN-Q

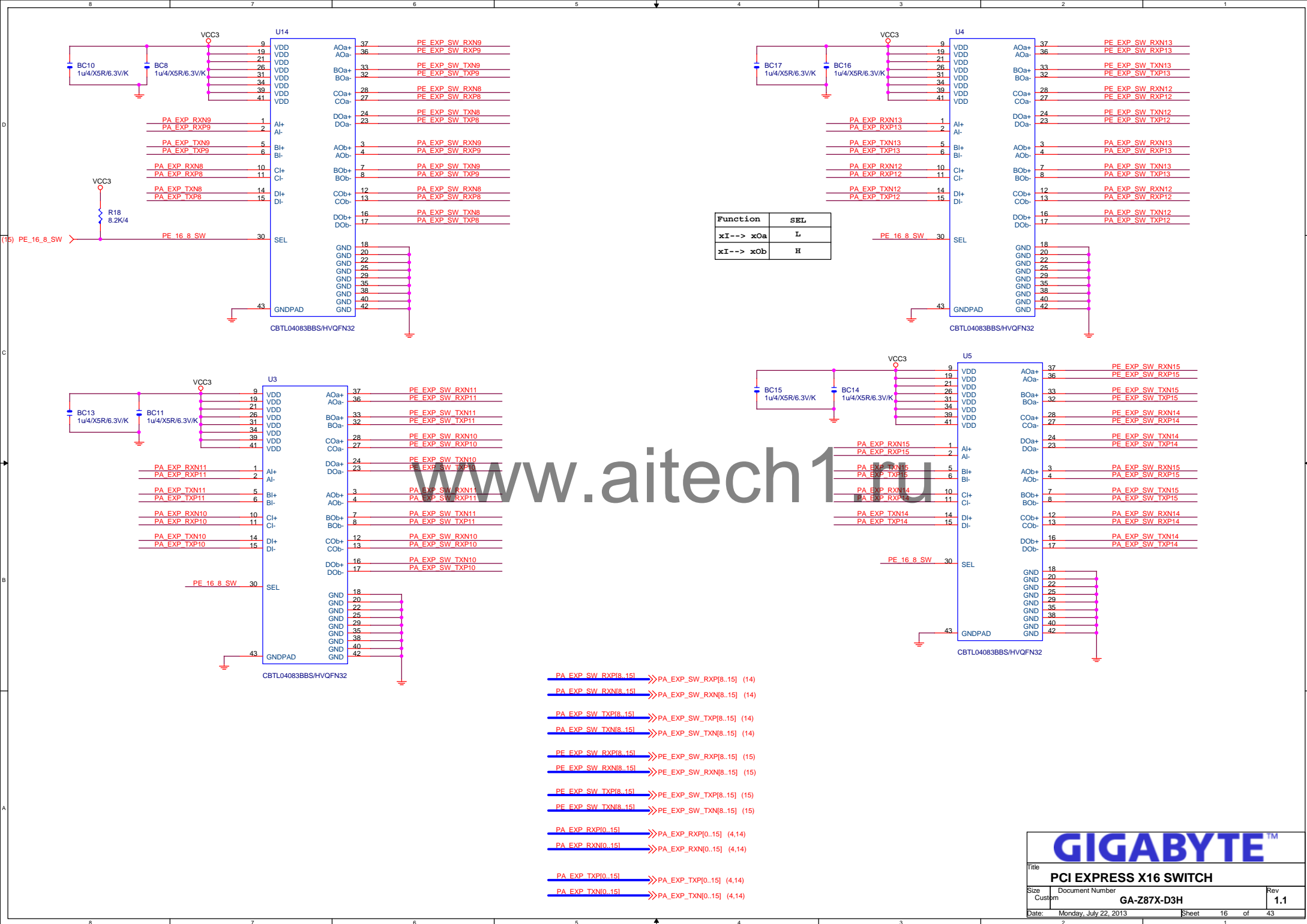


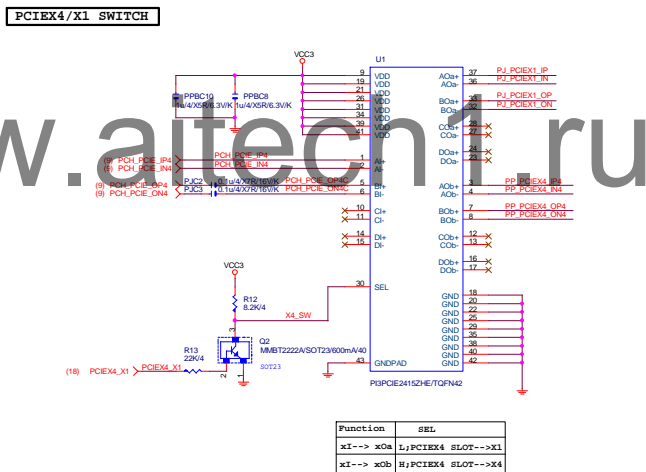
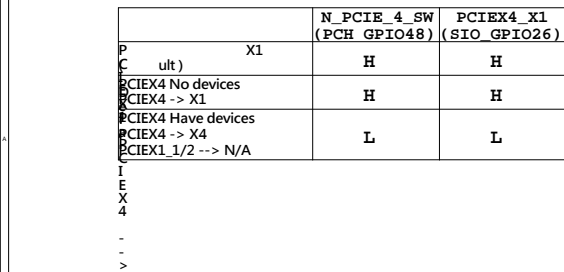
PCI-E/16x-164P/BK/LONG DOUBLE

Gigabyte Technology

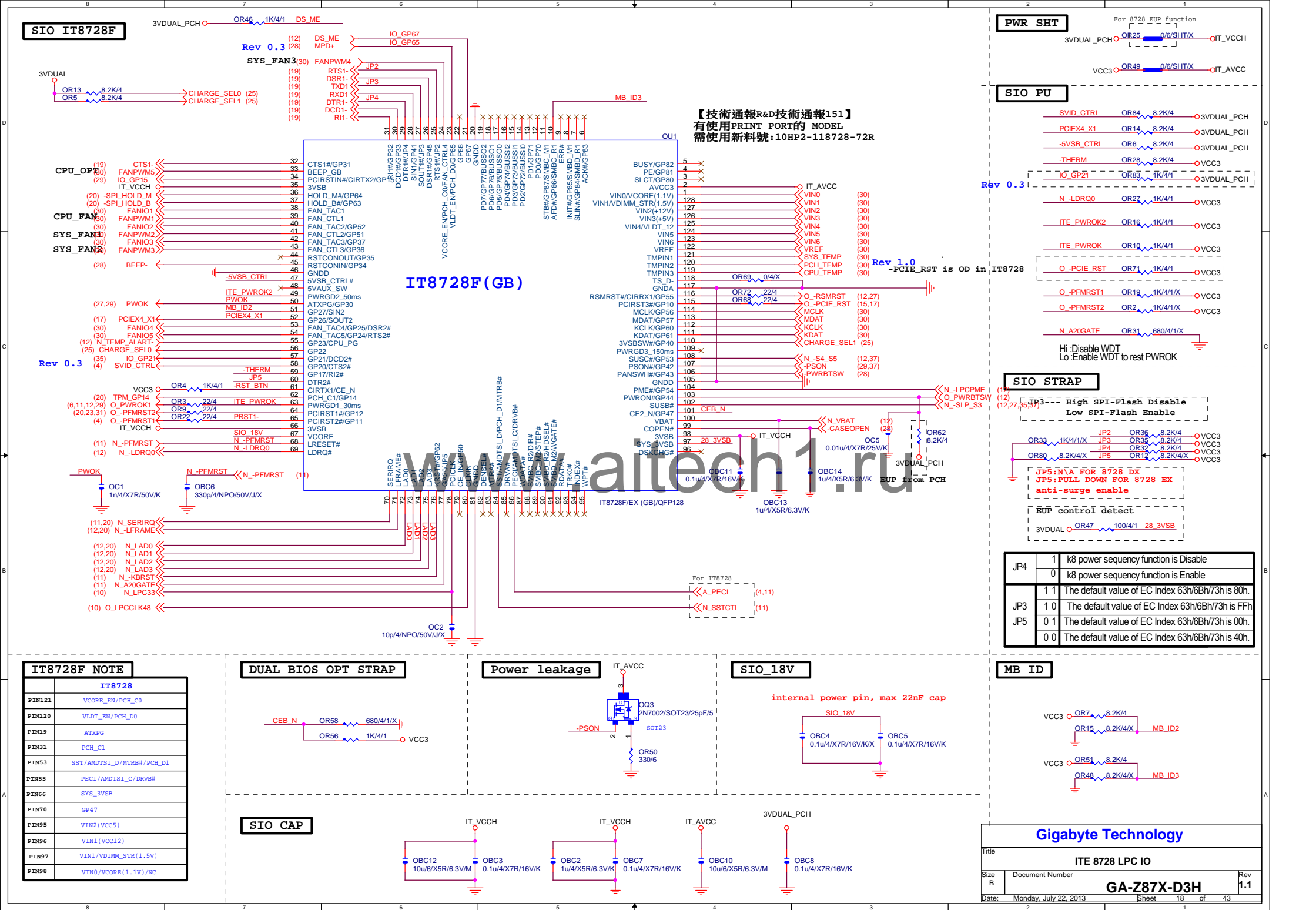
Title			
PCI EXPRESS * 16			
Size			
Document Number			
GA-Z87X-D3H			
Rev			
1.1			
Date:			
Monday, July 22, 2013			
Sheet			
14 of 43			



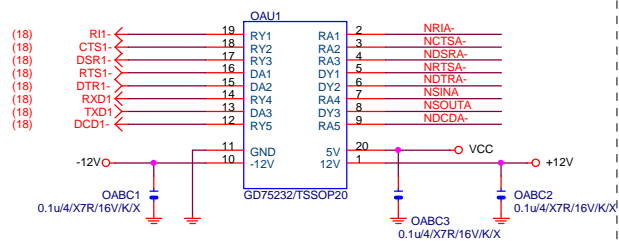




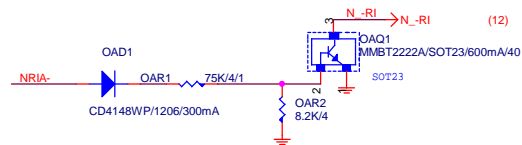
Gigabyte Technology			
Title PCIE_X1 1,2			
Size Custom	Document Number GA-Z87X-D3H		Rev 1.1
Date:	Monday, July 22, 2013	Sheet 17	of 43



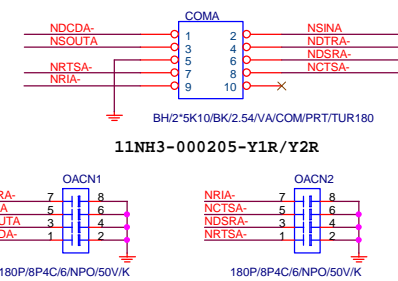
COMA



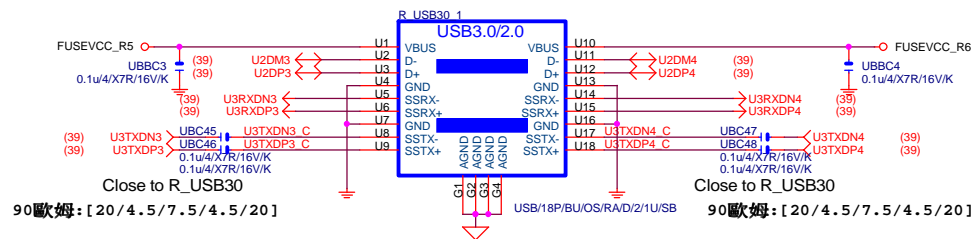
COM RI



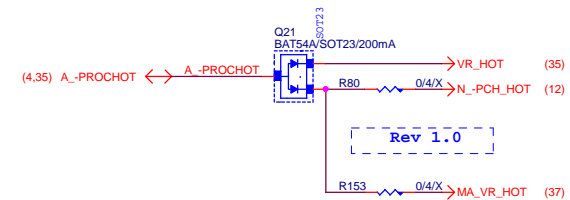
COM BUFFER



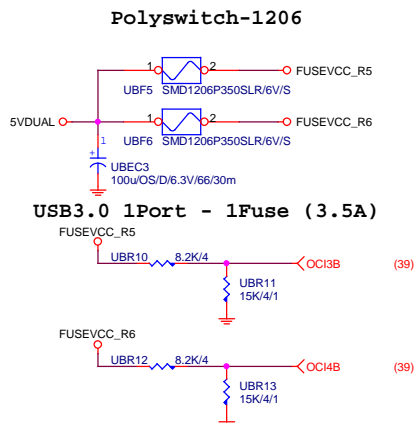
USB30_20 CONNECT



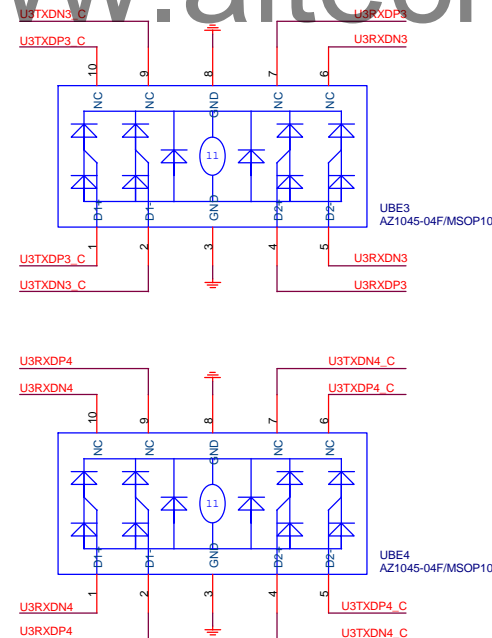
-PROHOT



USB30 PWR

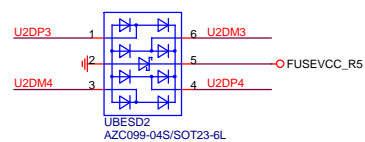


USB30 ESD PROTECT



-PROHOT

USB20 ESD PROTECT

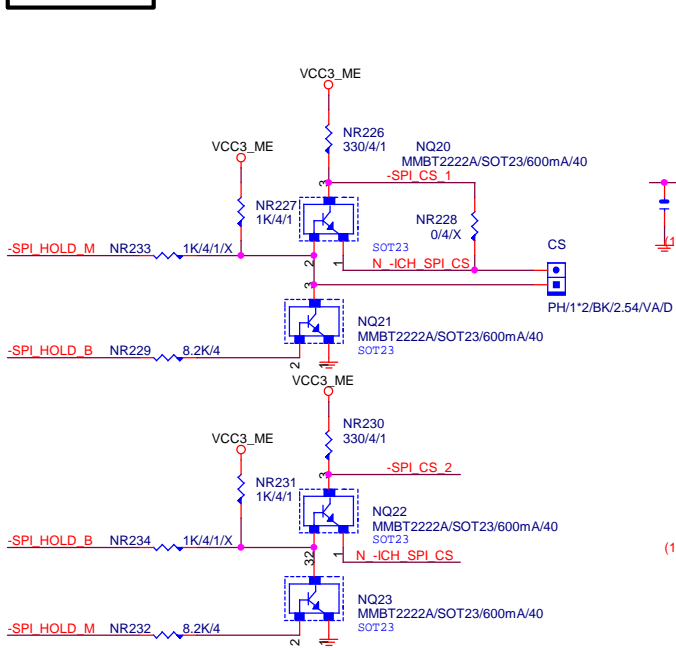


Gigabyte Technology

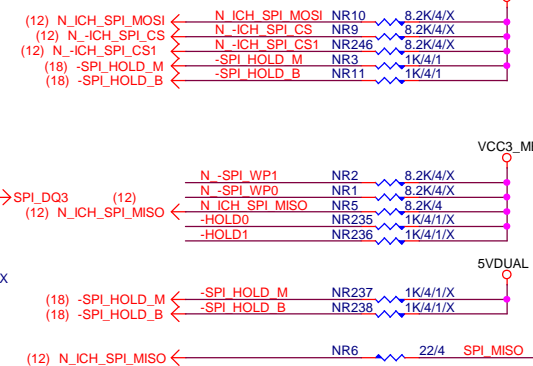
Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number	Rev	
Custpm		1.1	
Date:	Monday, July 22, 2013	Sheet	19 of 43

GA-Z87X-D3H

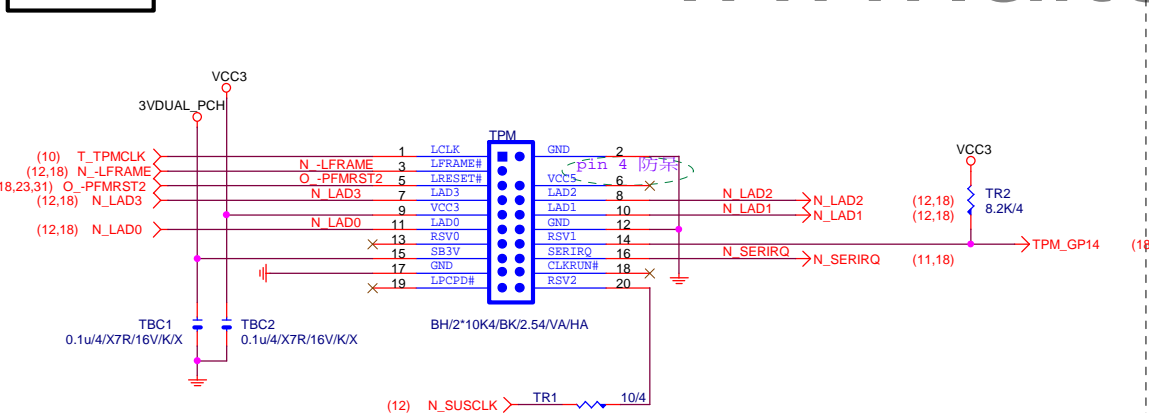
DUAL BIOS



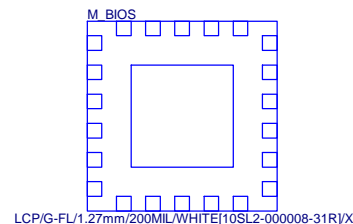
MOSI For DMI RX Termination Voltage



TPM CONNECT



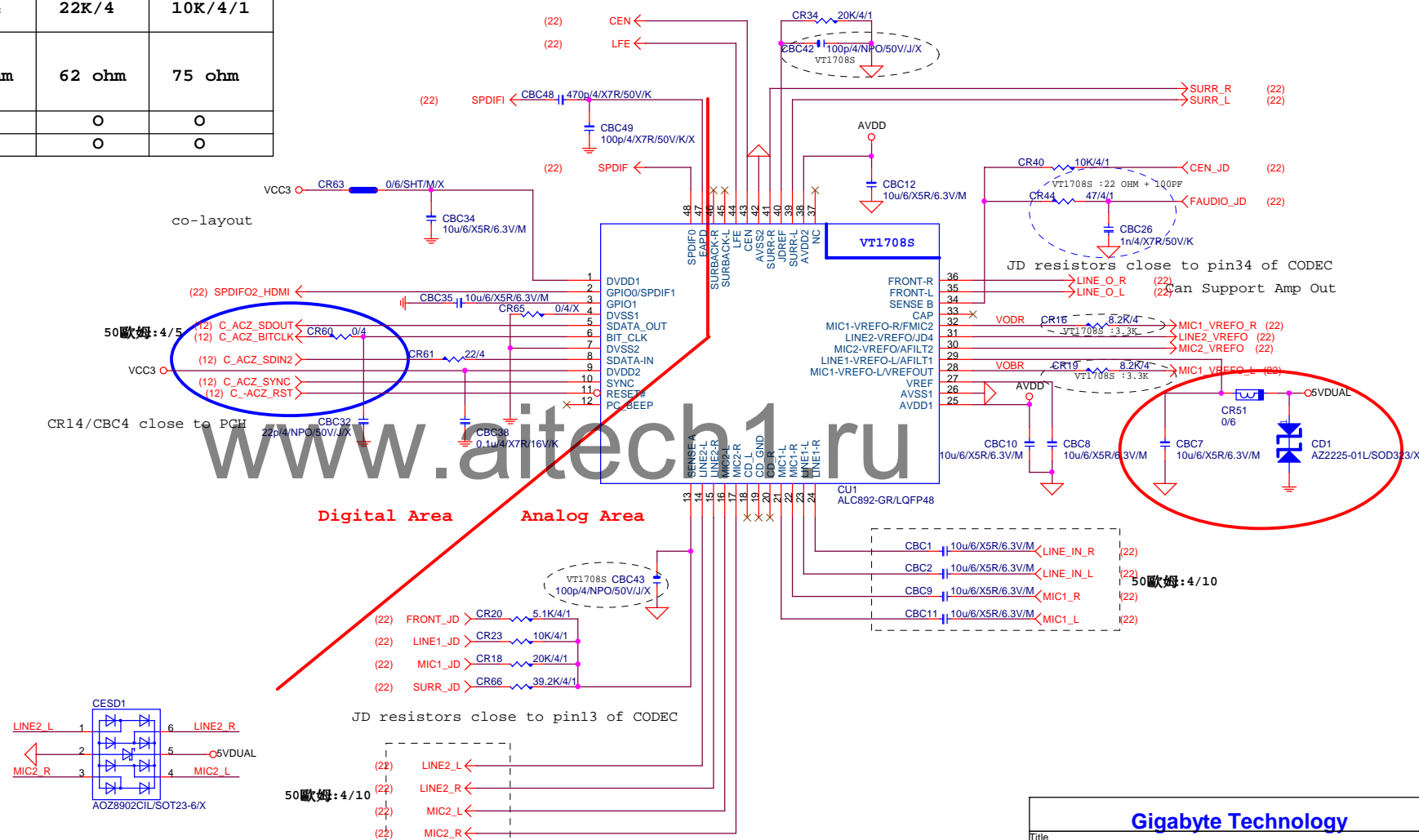
BIOS Debug port



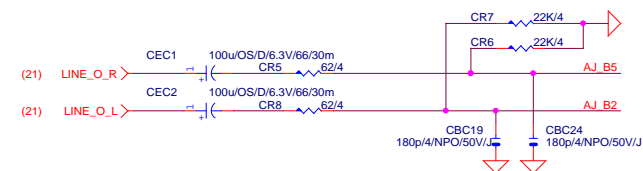
Gigabyte Technology

Title			BIOS
Size	Document Number	GA-Z87X-D3H	
Custom		Rev	1.1
Date:	Monday, July 22, 2013	Sheet	20 of 43

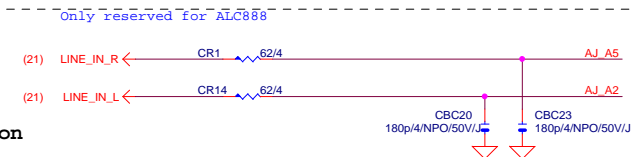
	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O



LINE-OUT



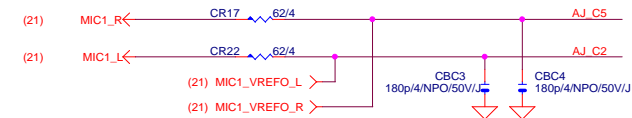
LINE-IN



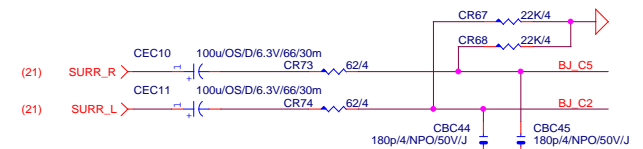
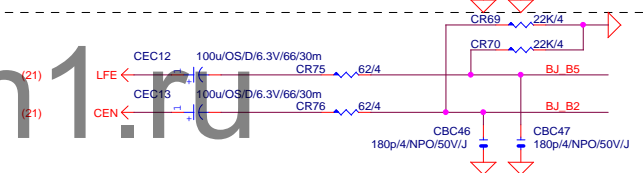
Verify MIC function
in LINE-in

For 889A/888

MIC-IN

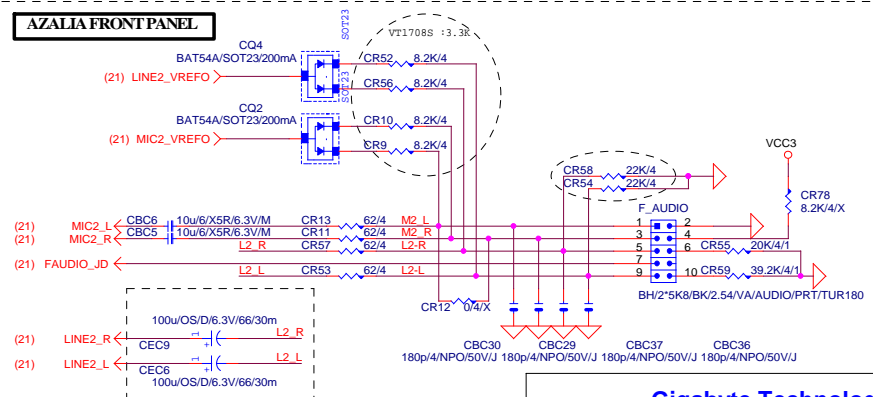


SURROUND

**CEN/LFE**

SURR BACK

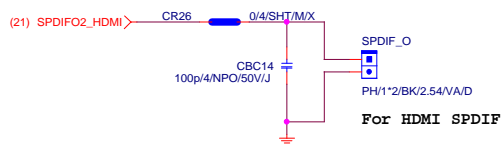
AZALIA FRONT PANEL



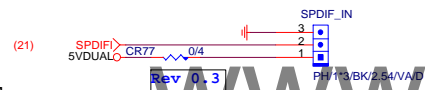
Gigabyte Technology

Title			
AUDIO JACK			
Size Custom	Document Number	GA-Z87X-D3H	Rev 1.1
Date: Monday, July 22, 2013	Sheet	22 of 43	

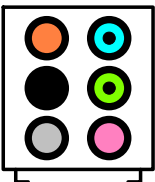
SPDIF_OUT



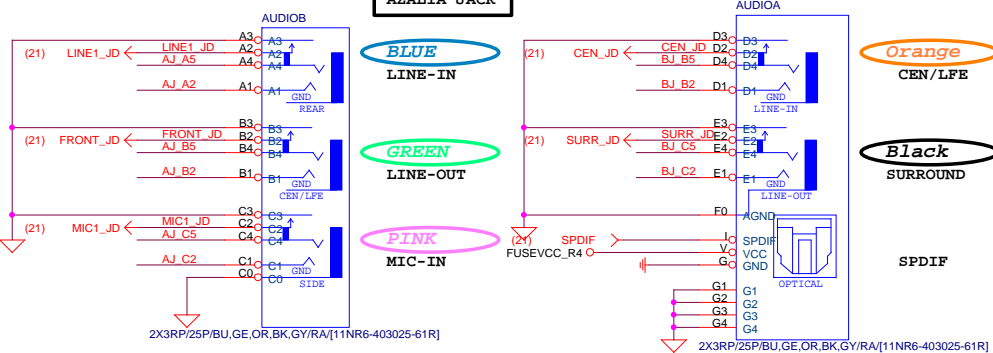
SPDIF_IN

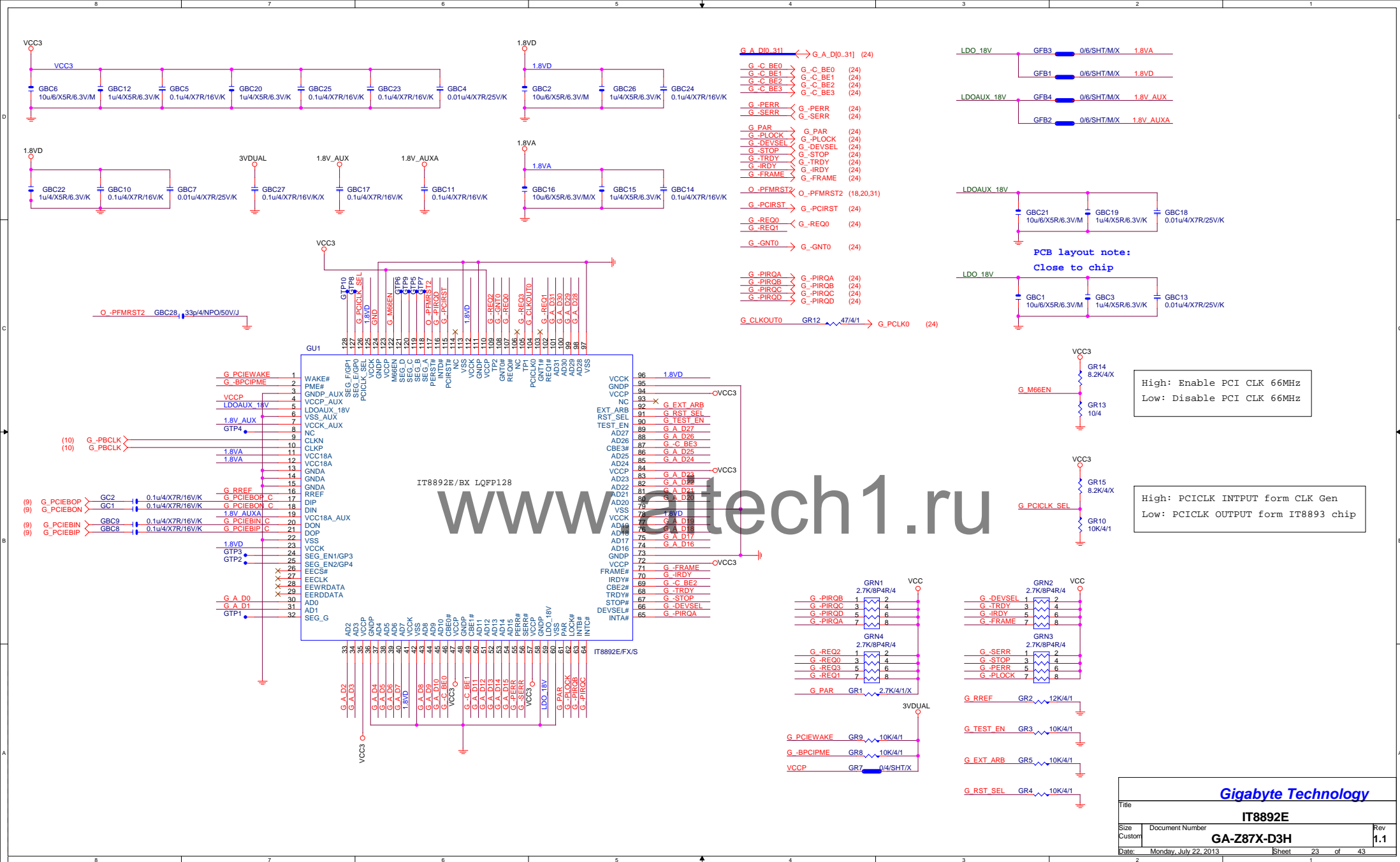


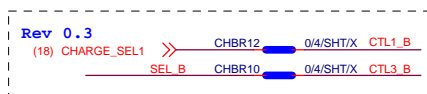
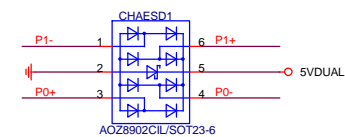
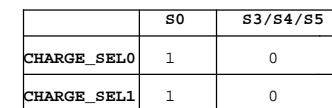
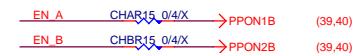
AZALIA JACK



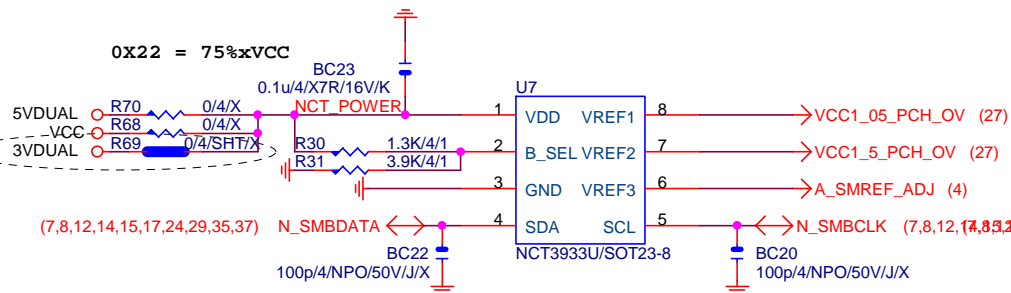
AZALIA JACK



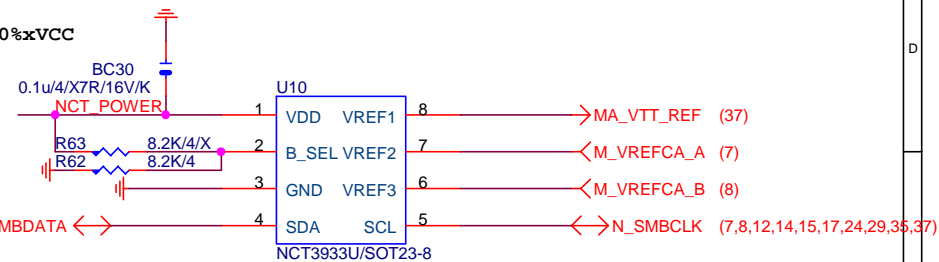




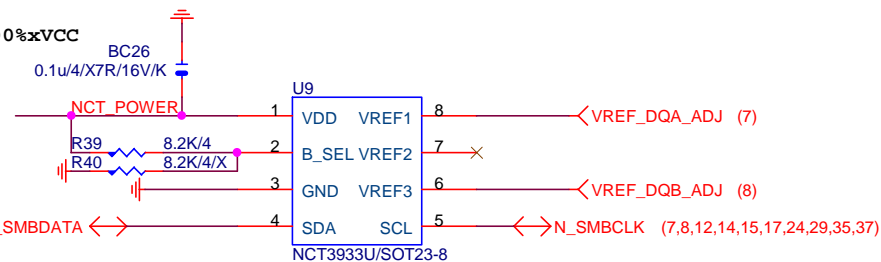
OVER VOLTAGE



0X2A = 0%xVCC



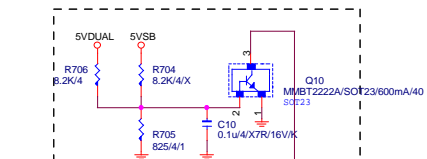
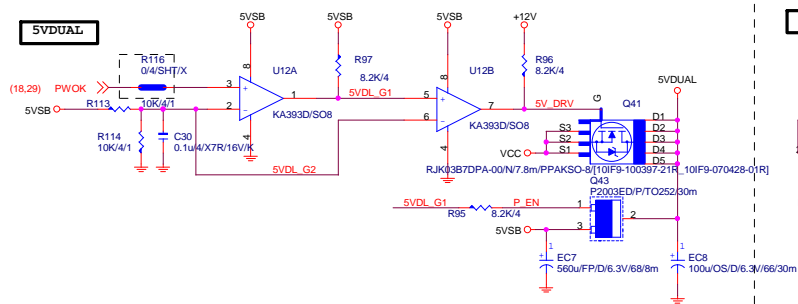
0X20 = 100%xVCC



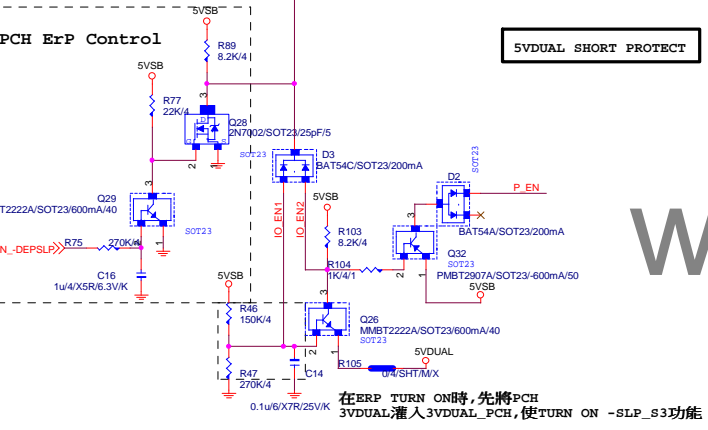
NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology

Title		
CPU CORE VR-2		
Size	Document Number	Rev
Custom	GA-Z87X-D3H	1.1
Date:	Monday, July 22, 2013	Sheet 26 of 43



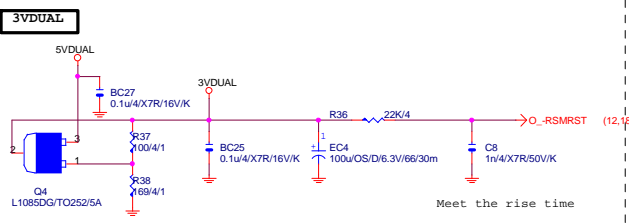
5VSB OVP: 7.5V protection



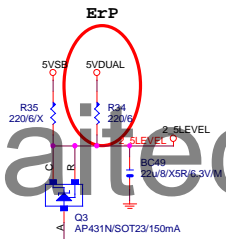
PCH ErP Control

5VDUAL SHORT PROTECT

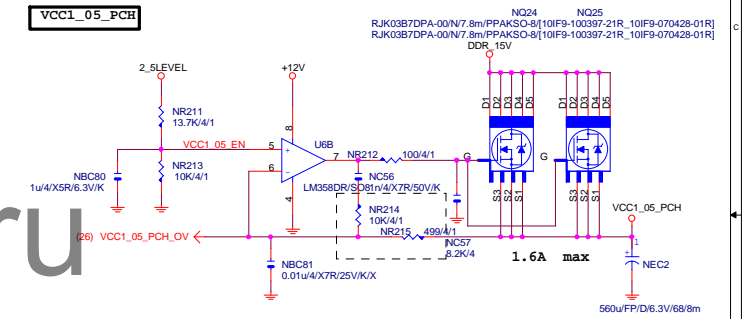
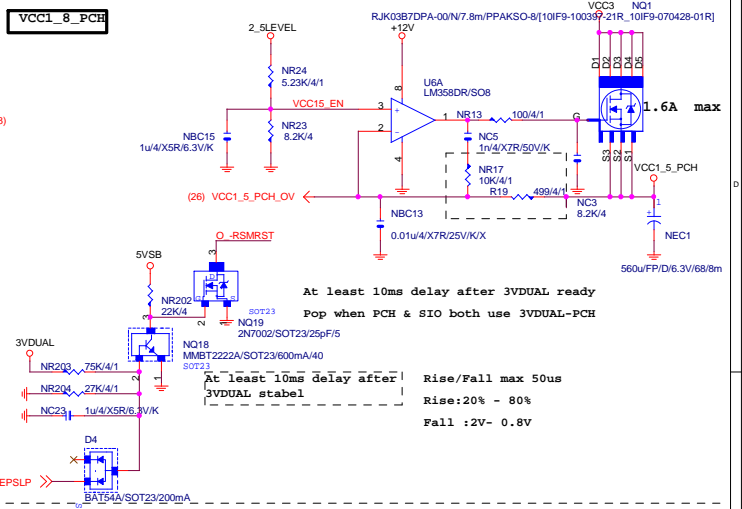
在ERP TURN ON時, 先將PCH 3VDUAL灌入3VDUAL_PCH, 使TURN ON -SLP_s3功能



2_5LEVEL

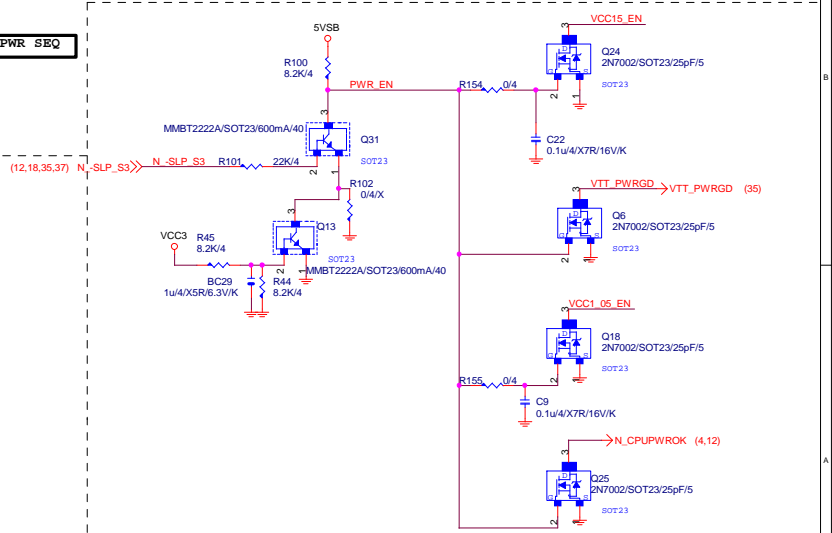


ErP

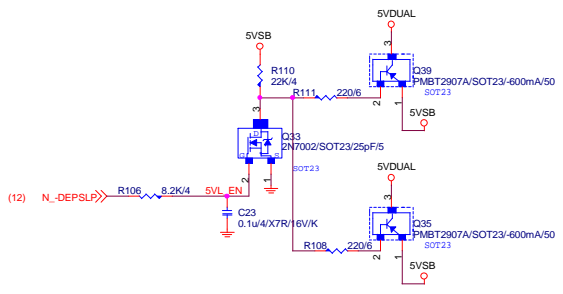
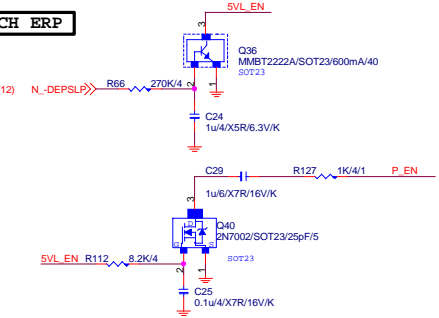


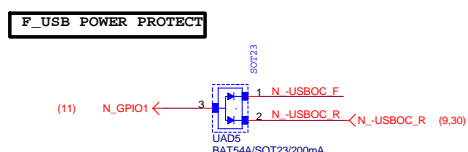
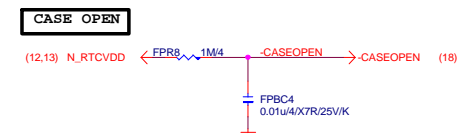
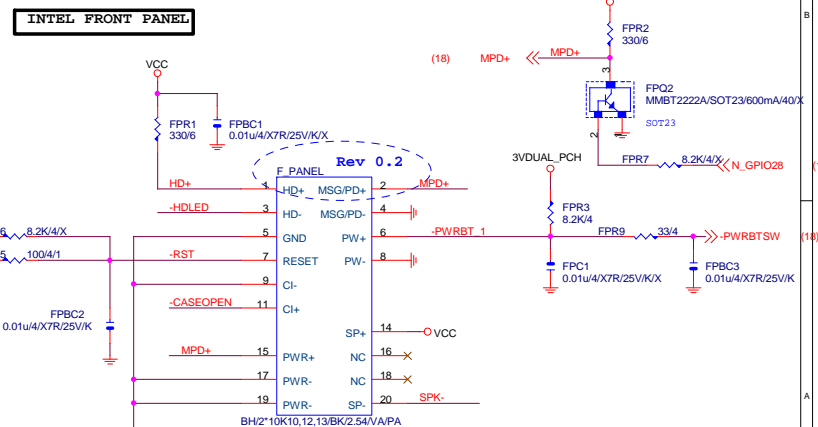
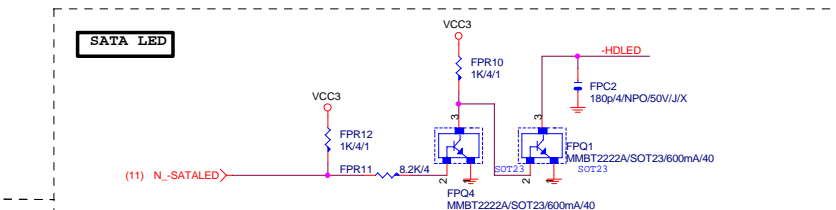
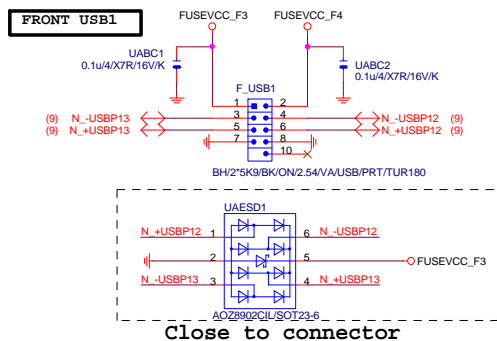
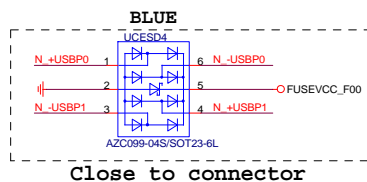
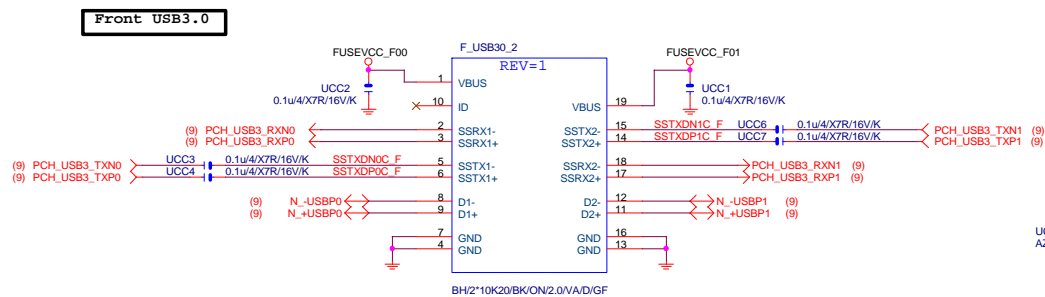
VCC1_05_PCH

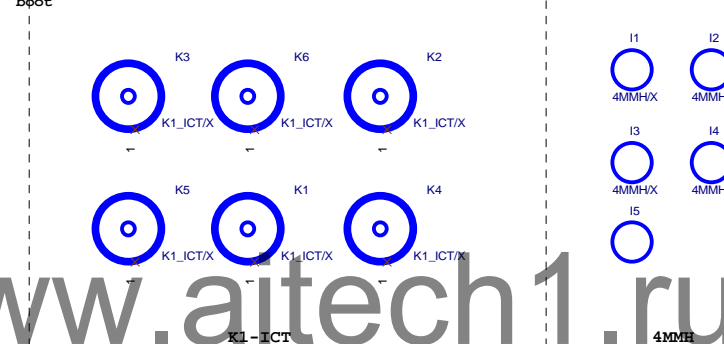
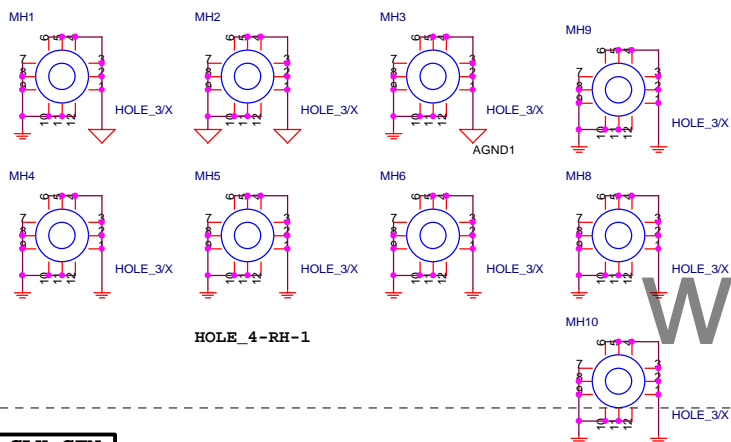
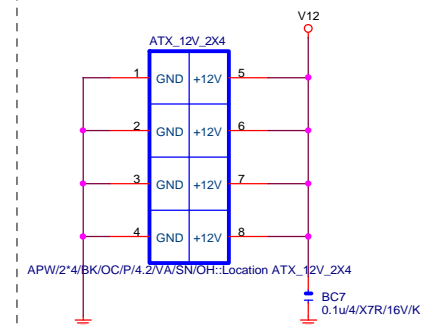
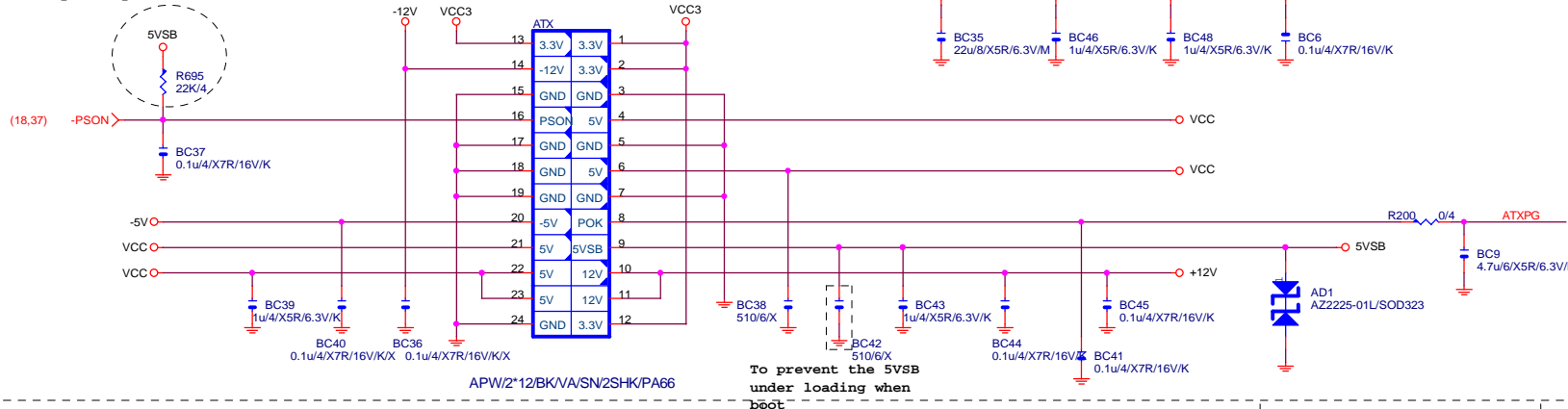
PWR SEQ



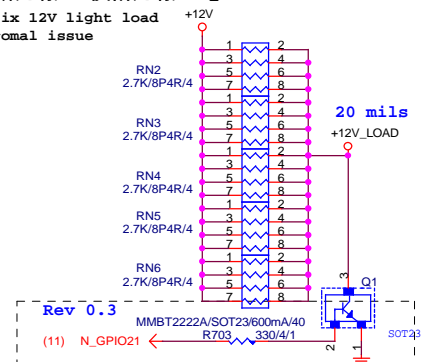
PCH ERP







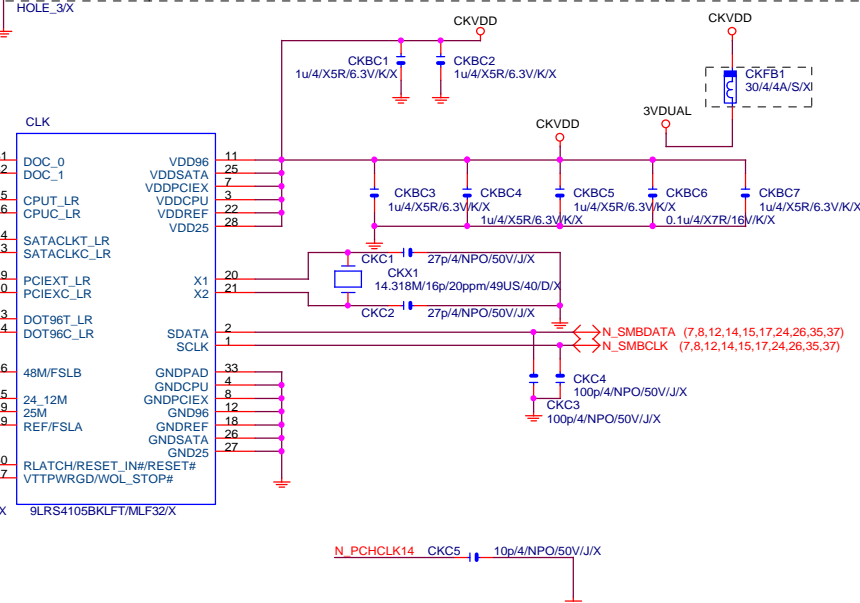
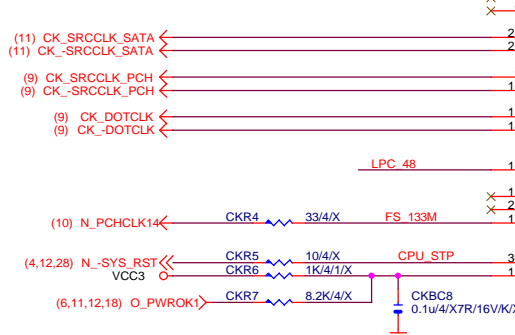
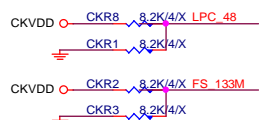
To fix 12V light load
abnromal issue



CLK GEN

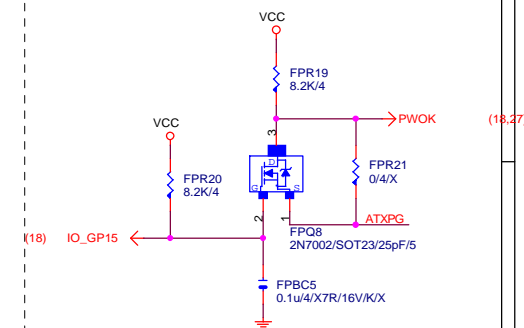
CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M



PWOK PATCH

【技術通報R&D技術通報154】

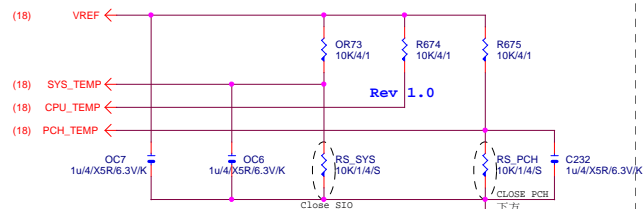


Gigabyte Technology

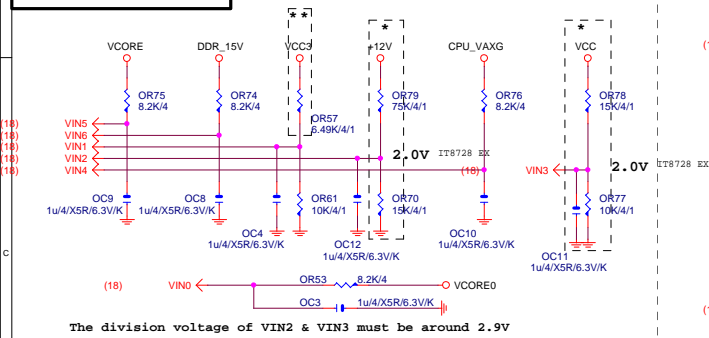
Title		ATX POWER CONNECTOR	
Size	Document Number	GA-Z87X-D3H	
Custom			

Re	1.1
----	-----

TEMP H/W MONITOR

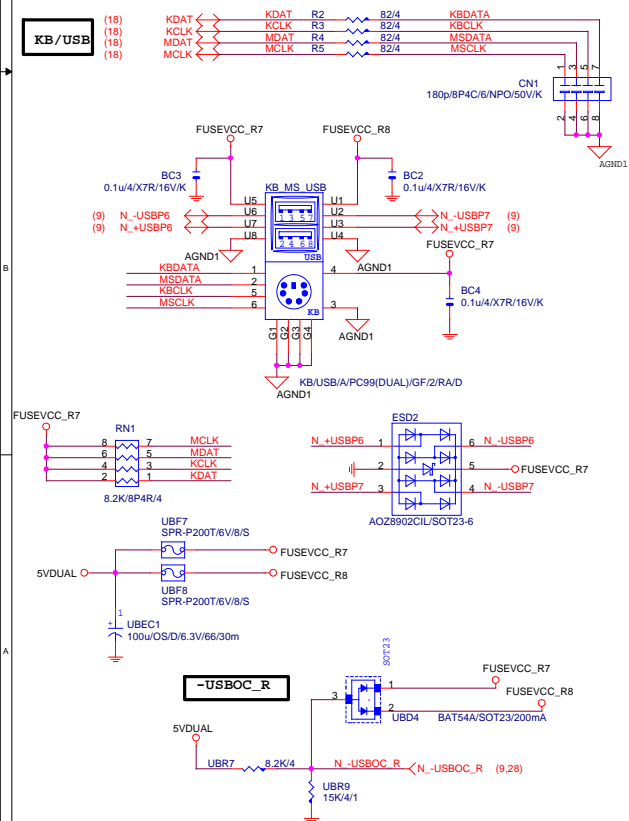


VOLTAGE-- H/W MONITOR

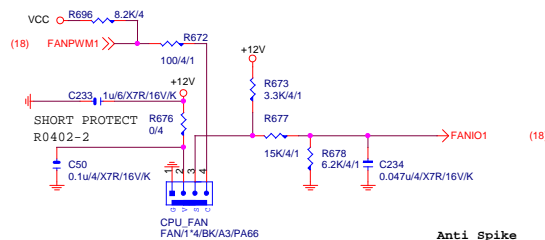


The division voltage of VIN2 & VIN3 must be around 2.9V

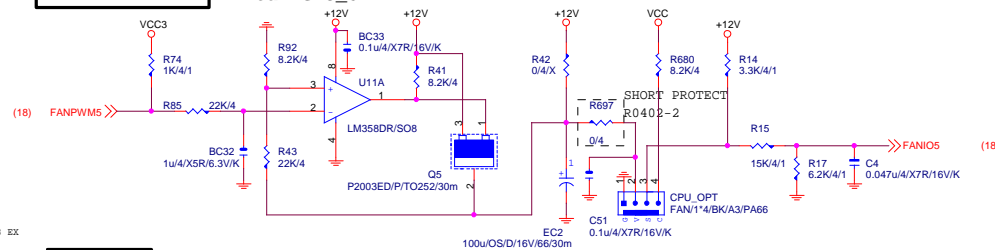
KB/USB



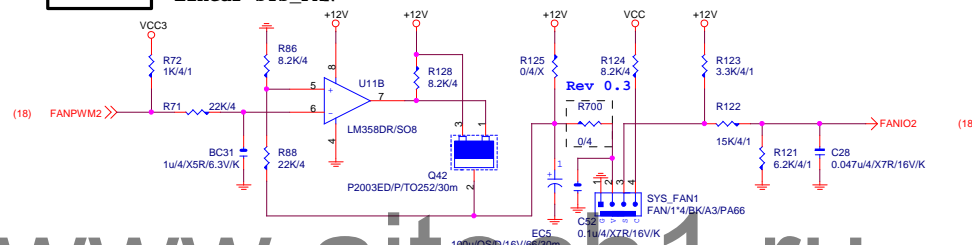
CPU SMART FAN



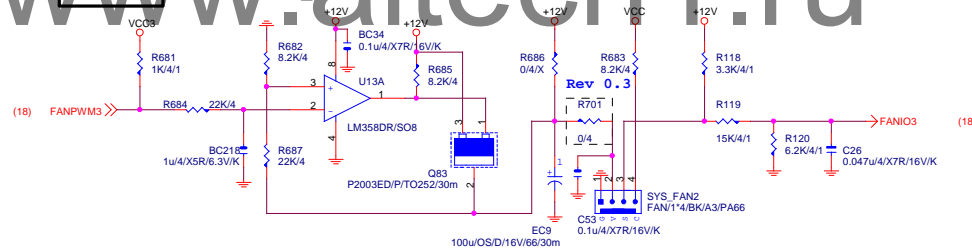
```
CPU OPT SMART FAN Linear CPU_OPT
```



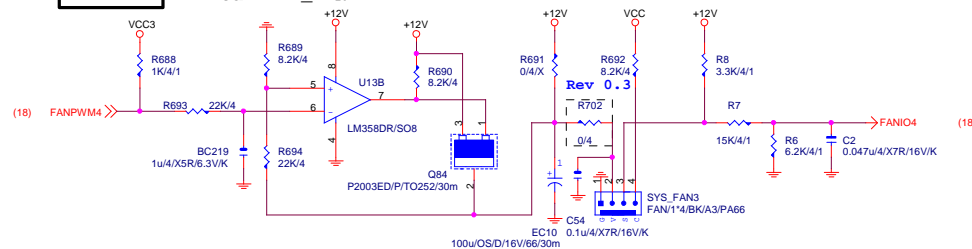
SYS_FAN_1 Linear SYS_FAN



SYS_FAN_2 Linear SYS_FAN



SYS_FAN_3 Linear SYS_FAN



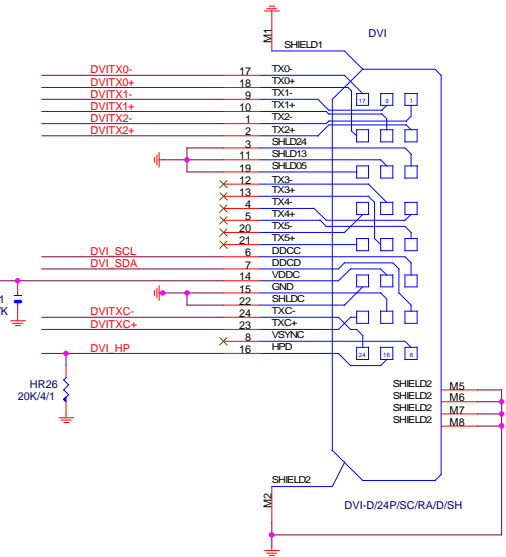
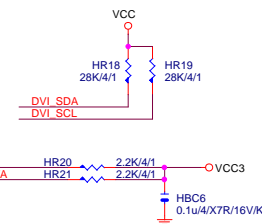
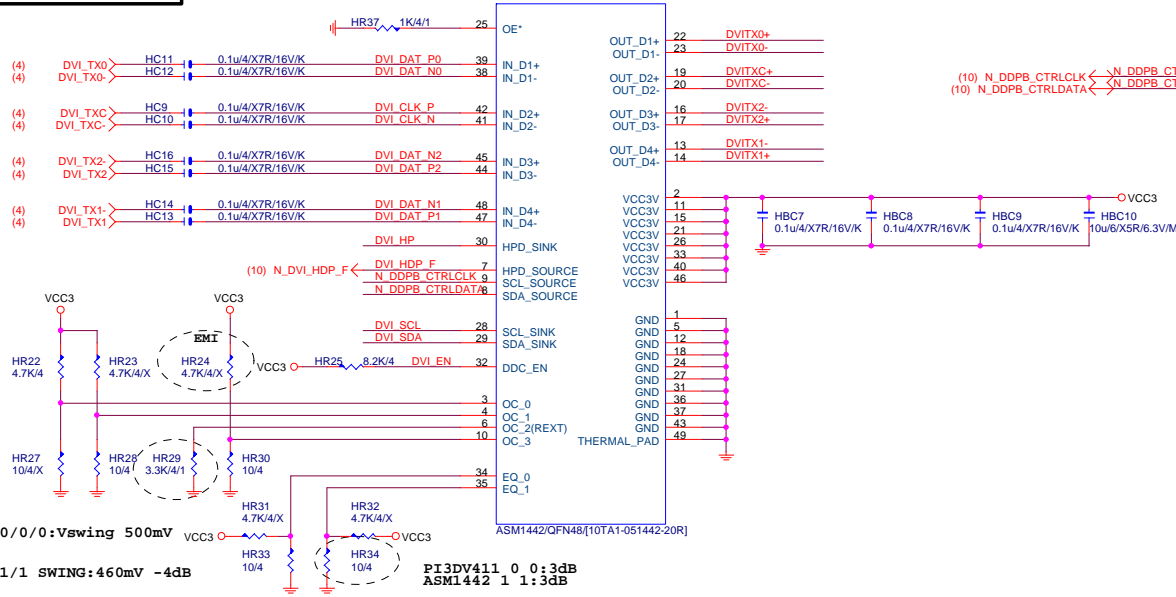
Gigabyte Technology

Title				HWM,KB/MS, FAN CTRL			
Size	Custom	Document Number					Rev
		GA-Z87X-D3H					1.1
Date:	Monday, July 22, 2013			Sheet	30	of	43

DVI LEVEL SHIFT

DVI:15/4/4/4/15

Impedance=85 +- 17.5%



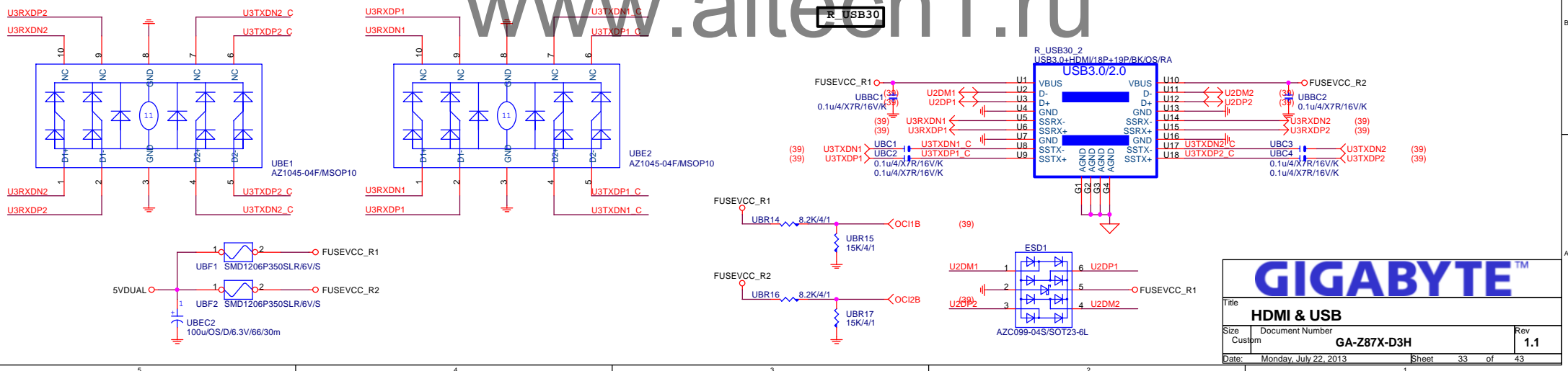
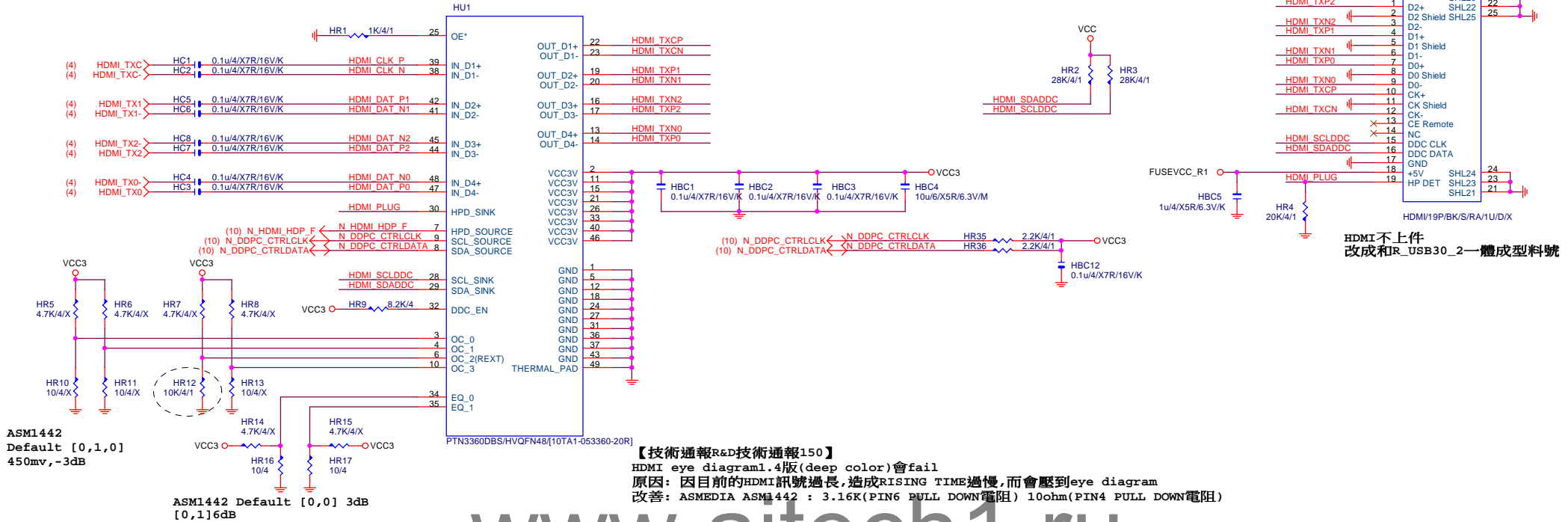
www.aitech1.ru

Gigabyte Technology		
Title		
TI TSB43AB23 1394		
Size	Document Number	Rev
Custom	GA-Z87X-D3H	1.1
Date:	Monday, July 22, 2013	Sheet 32 of 43

HDMI LEVEL SHIFT

HDMI:15/4/4/4/15

Impedance=85 +- 17.5%



5

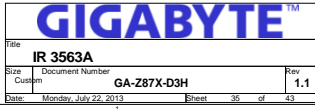


D

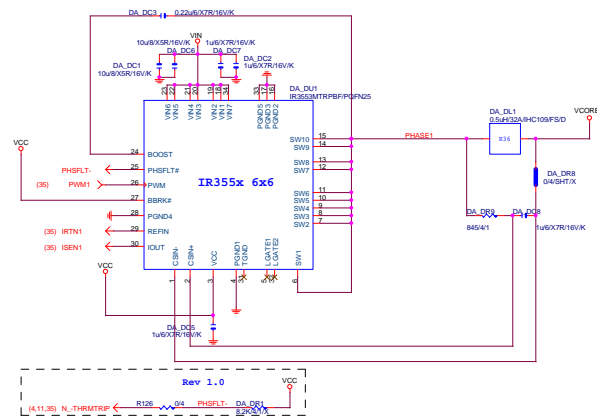
--	--

世

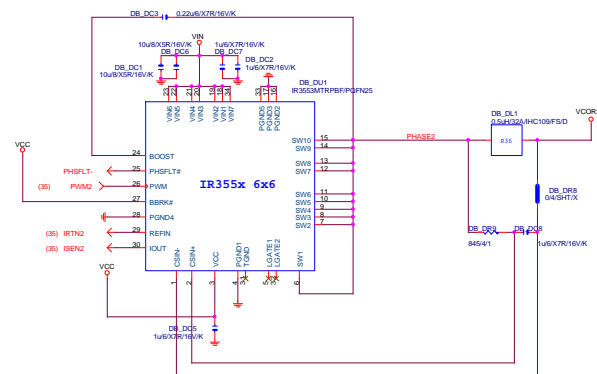
7.



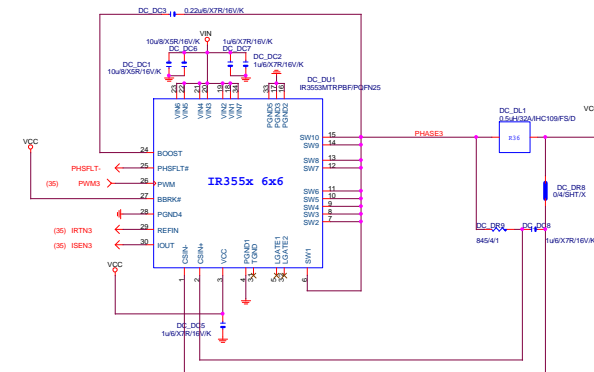
VCORE-PHASE1



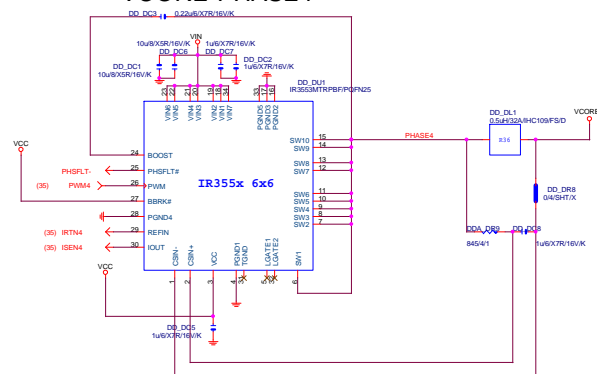
VCORE-PHASE2



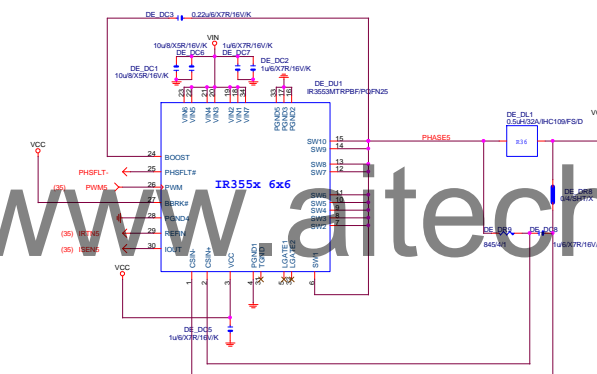
VCORE-PHASE3



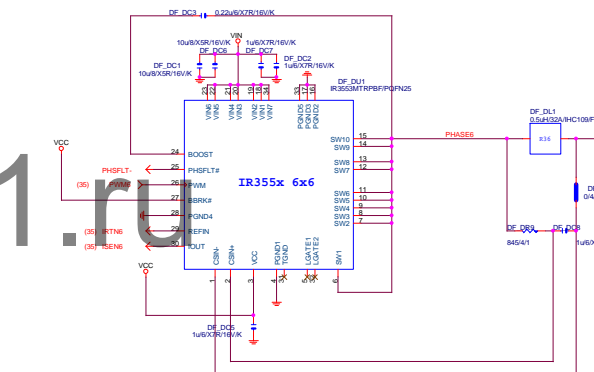
VCORE-PHASE4



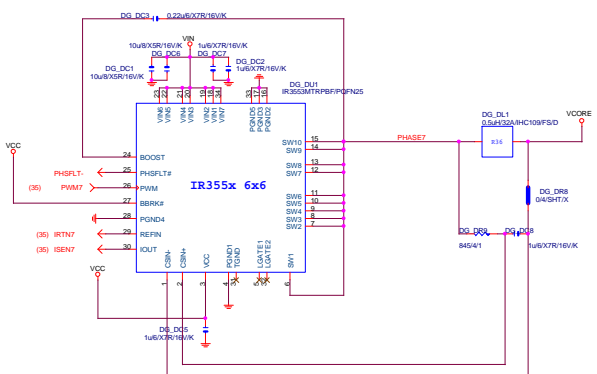
VCORE-PHASE5



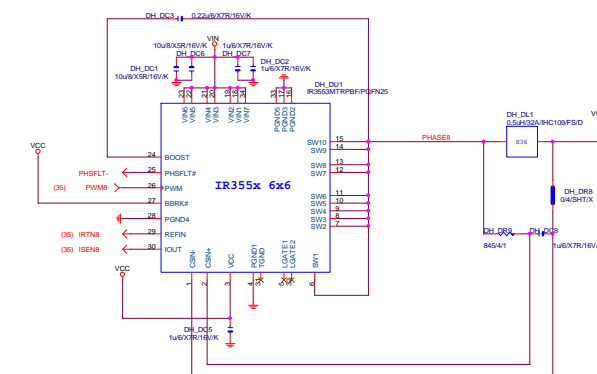
VCORE-PHASE6

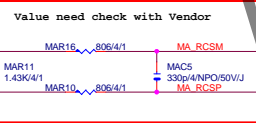
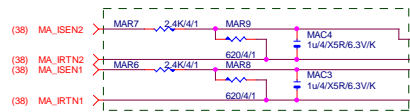
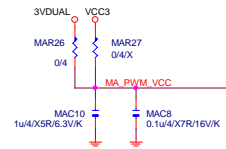
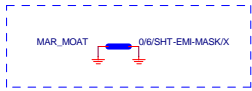


VCORE-PHASE7



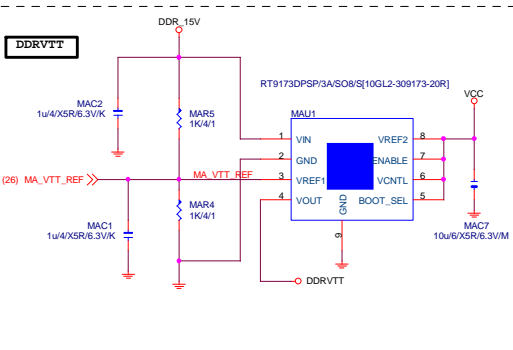
VCORE-PHASE8





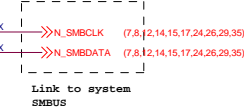
Close to DDR output inductor

should be routed as differential pair, 7mil width, 8mil spacing



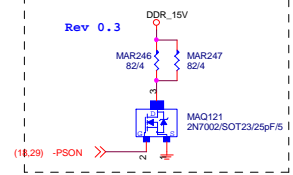
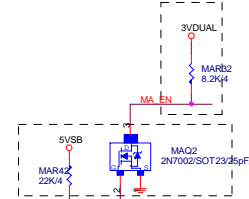
IR3570

MA_PWM2 (38)
MA_PWM1 (38)

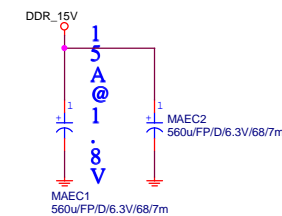
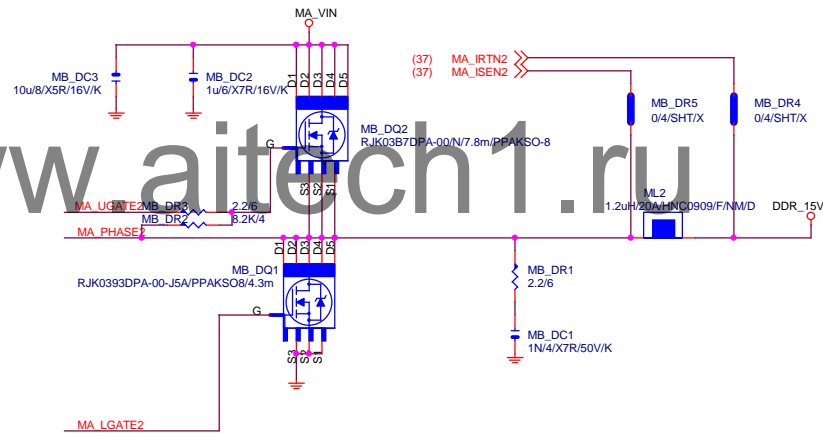
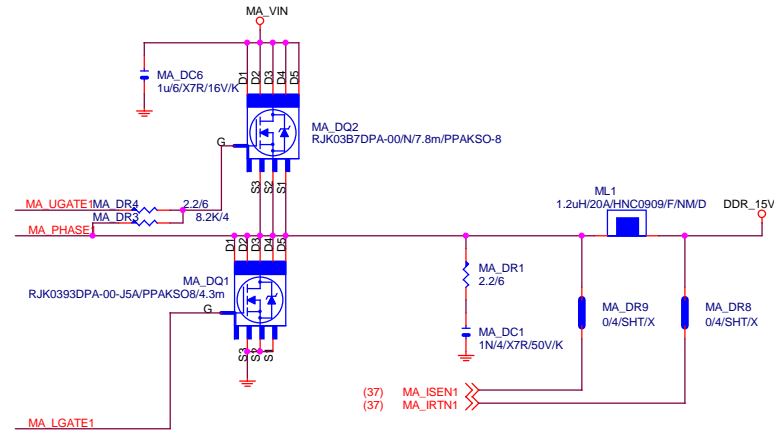
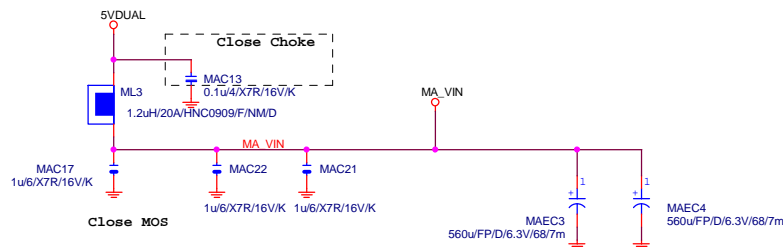
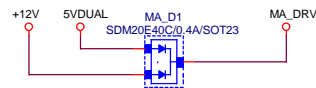
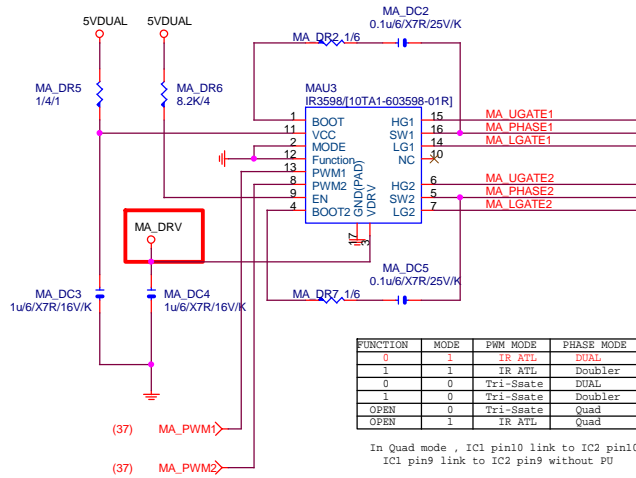


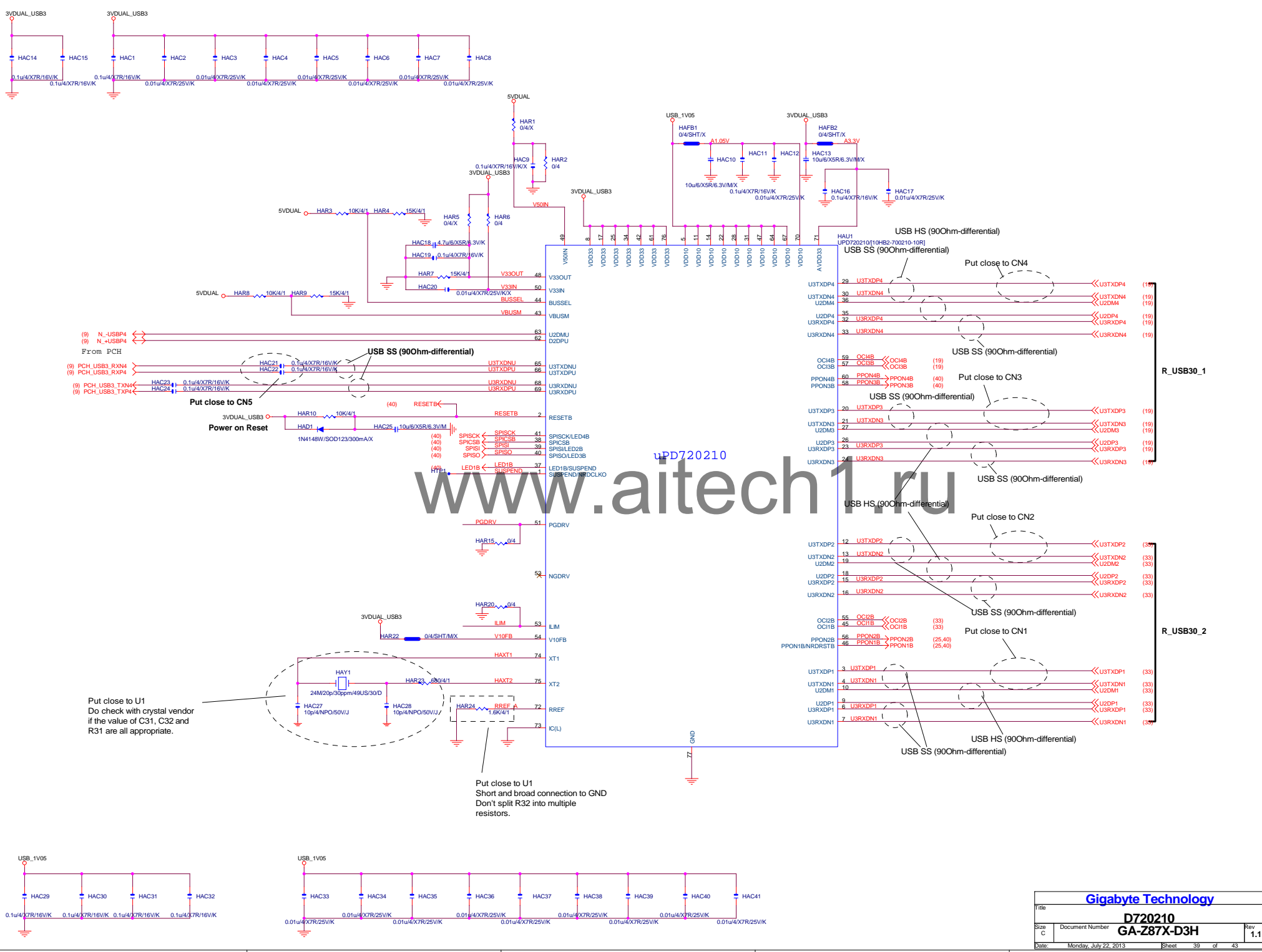
Addr: 74h

Link to PCH pin B046
Pull up in PCH side



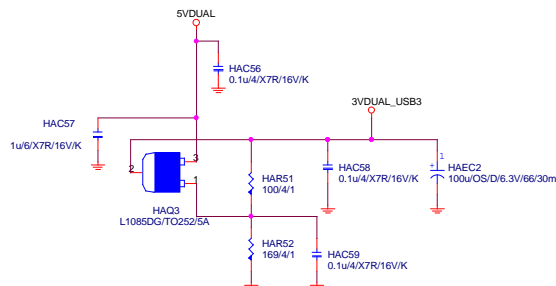
DDR_15V



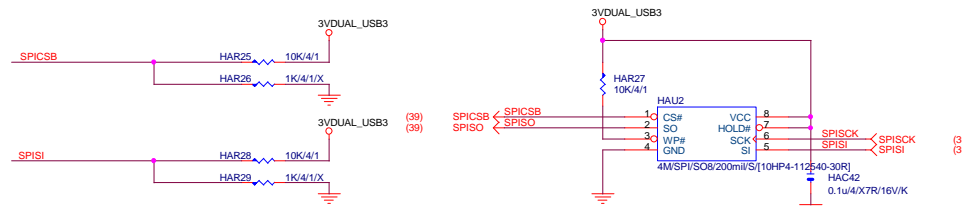


www.aitech1.ru

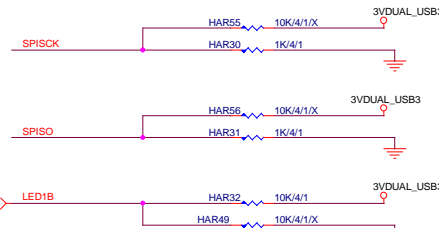
3VDUAL_USB_1



External SPI ROM ; SPI ROM attached mode

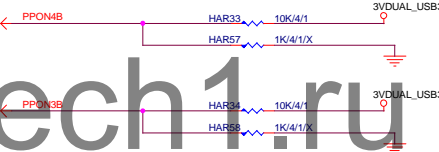


Battery Charging



Number of Ports ; 4Ports mode

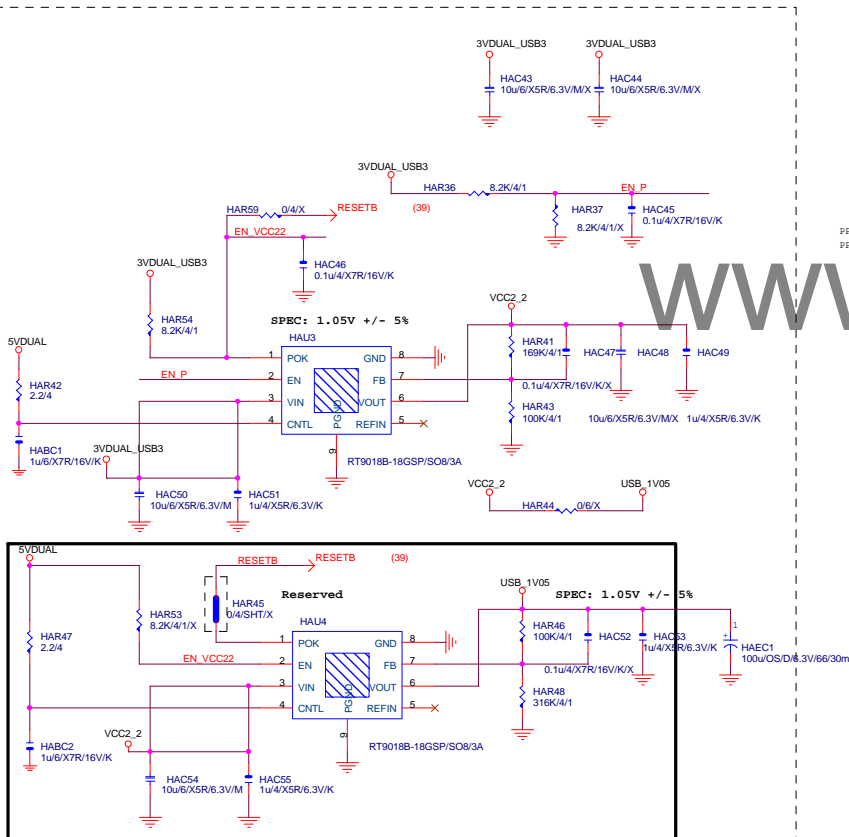
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)

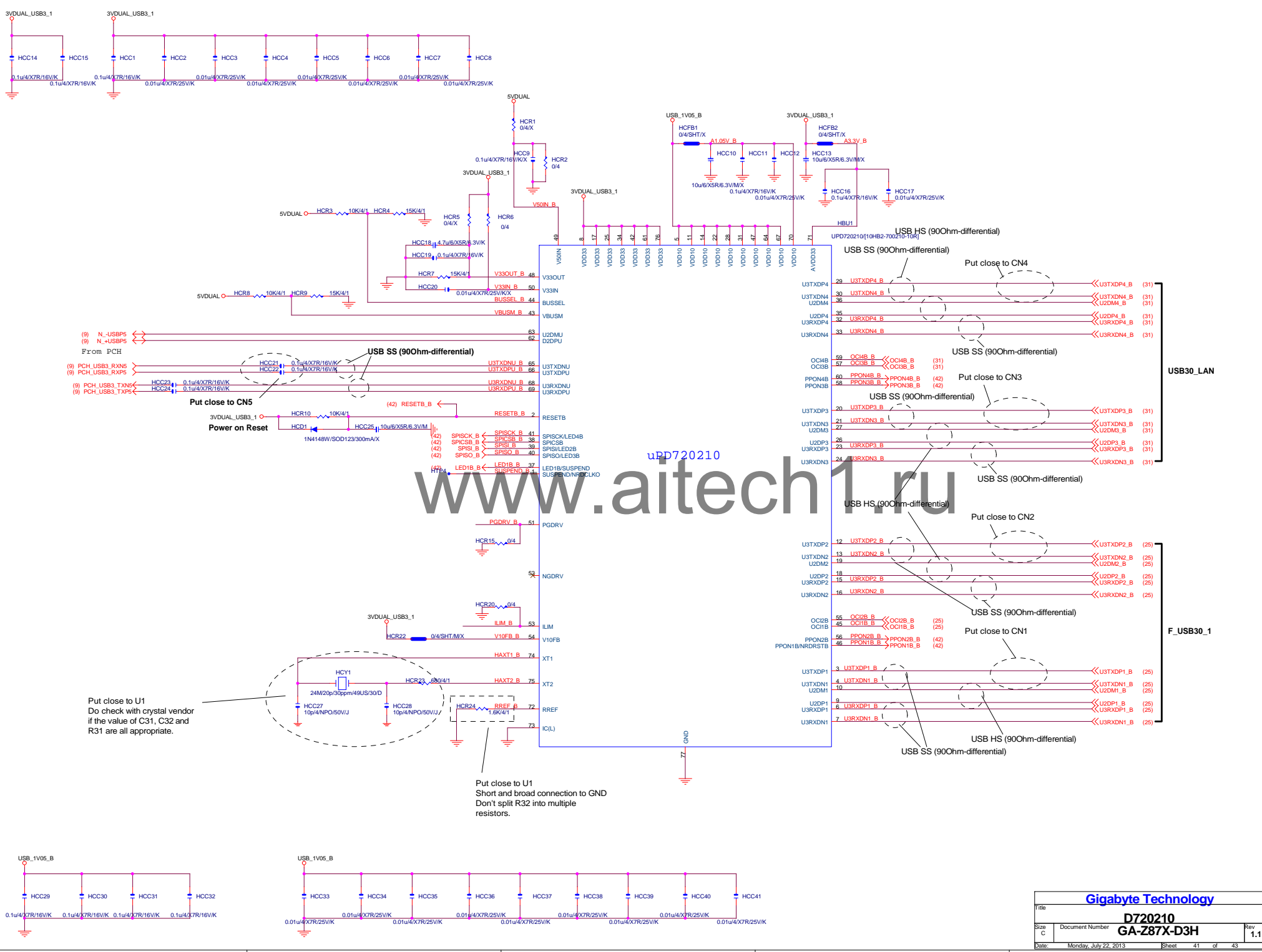


#5 VBUS Power Control ; Individual mode

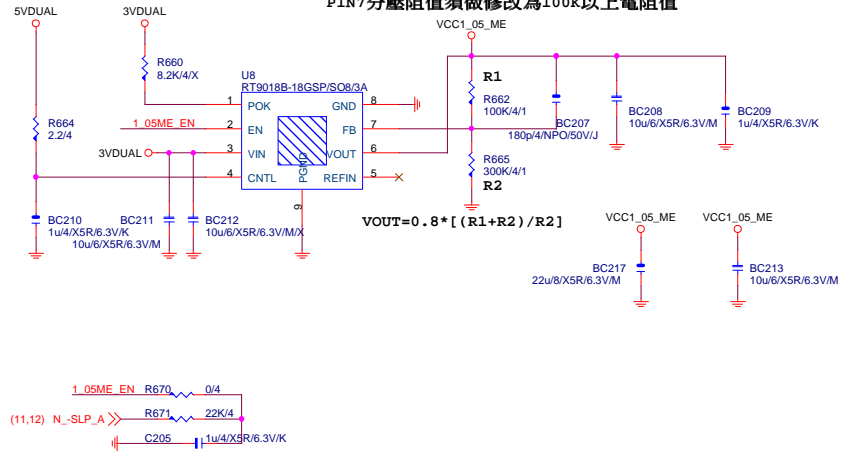


PPON1B Pin Function ; Port1 PPONB mode

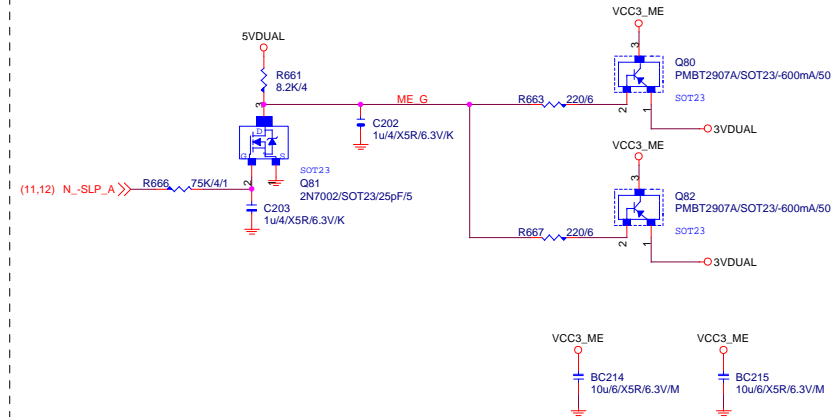




【技術通報R&D技術通報156】
(RICHTER), (NUVOTON), (EMC) 做共用
PIN7分壓阻值須做修改為100K以上電阻值



VCC3_ME



GIGABYTE™

Title		
RT8120_DDR_15V		
Size	Document Number	Rev
Custom	GA-Z87X-D3H	1.1
Date:	Monday, July 22, 2013	Sheet 43 of 43

www.aitech1.ru